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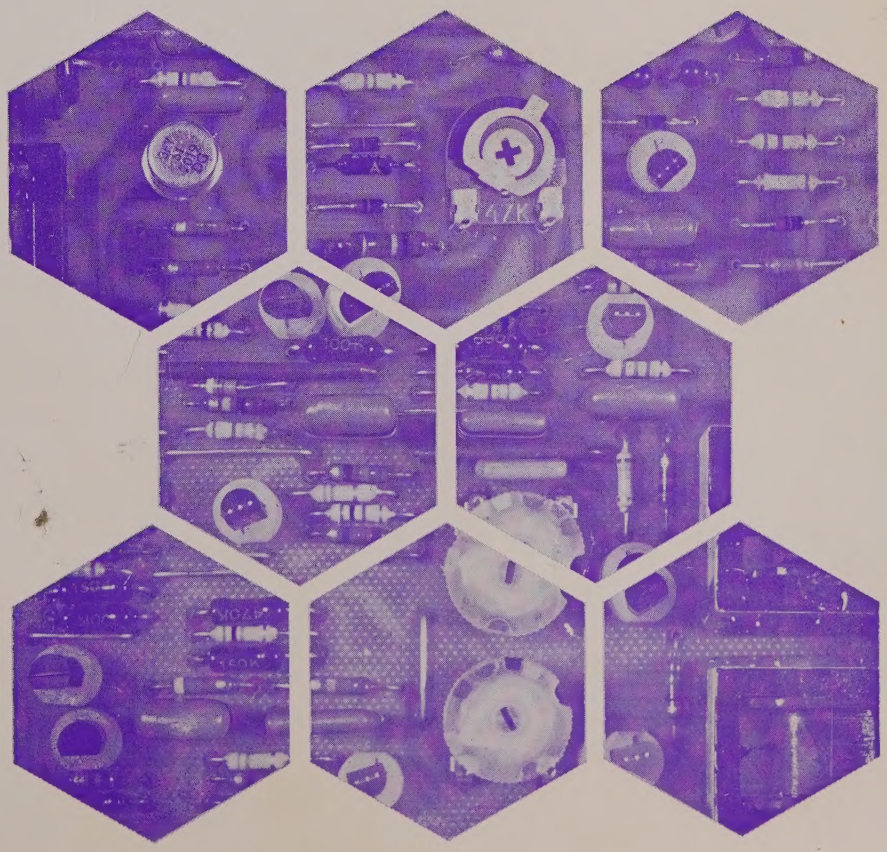
Temperature controllers type 017, 018, 020, 02

ISSUE 4



Temperature controllers type 017, 018, 020, 021

ISSUE 4

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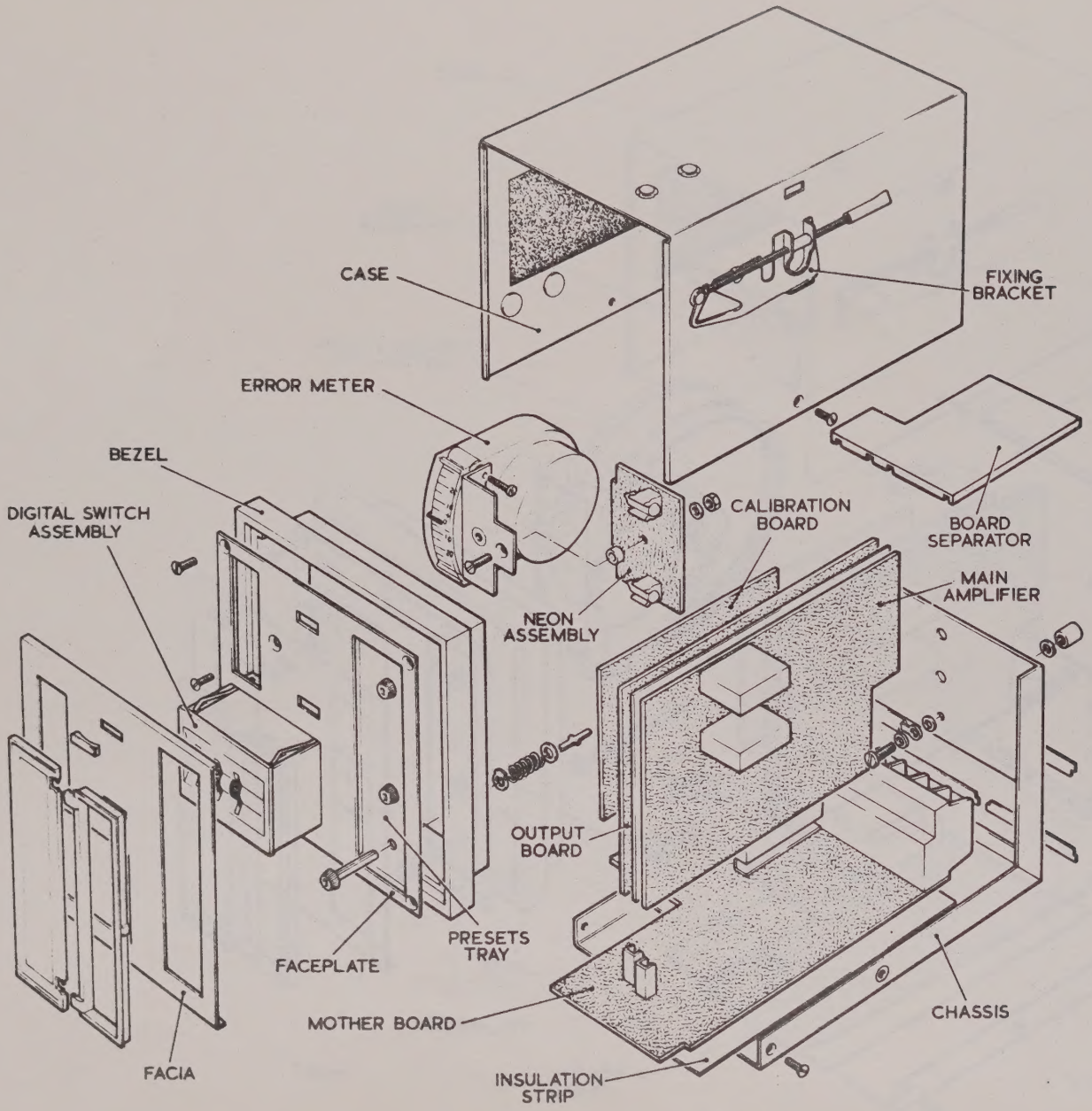
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FACIA
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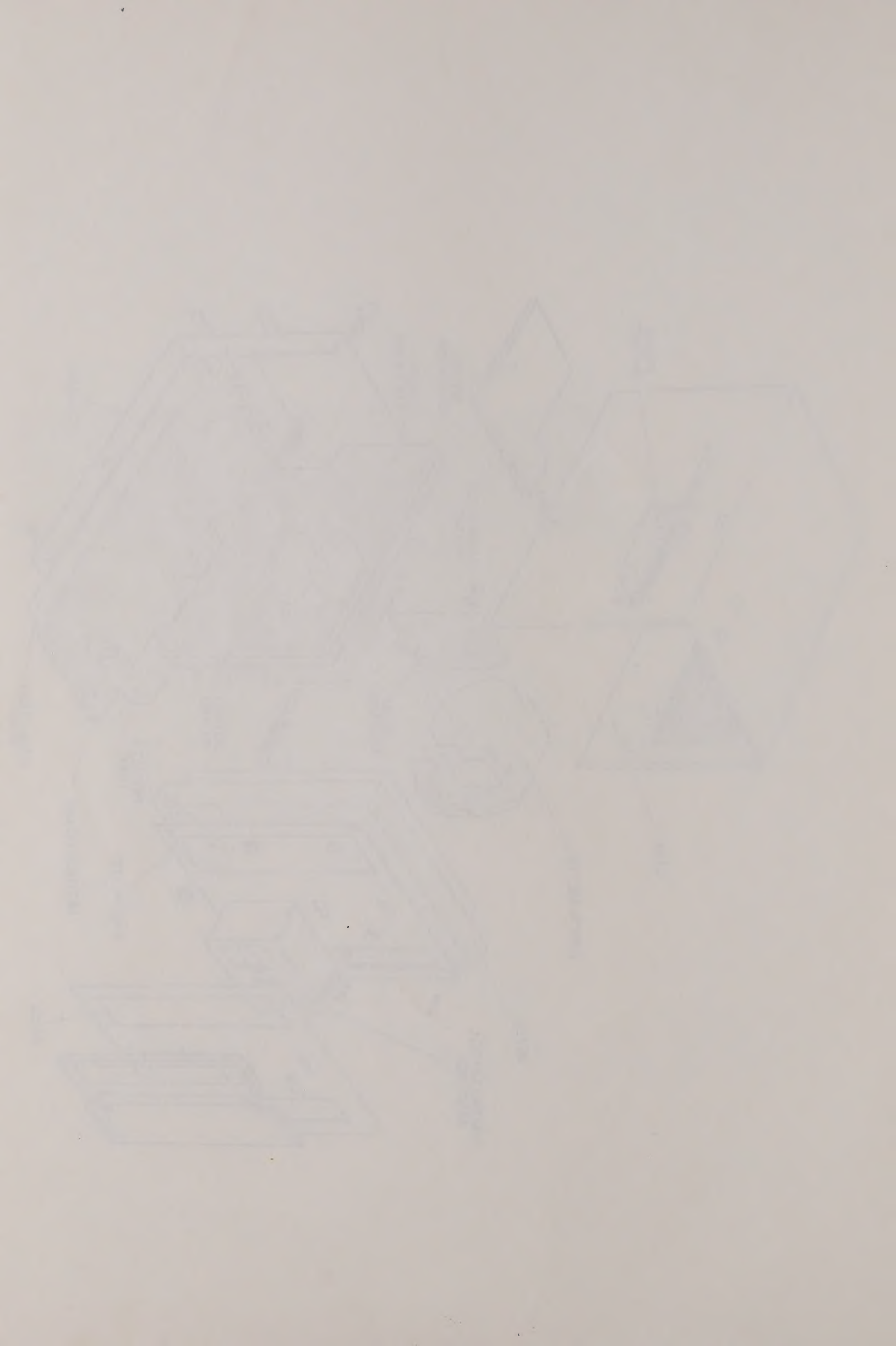

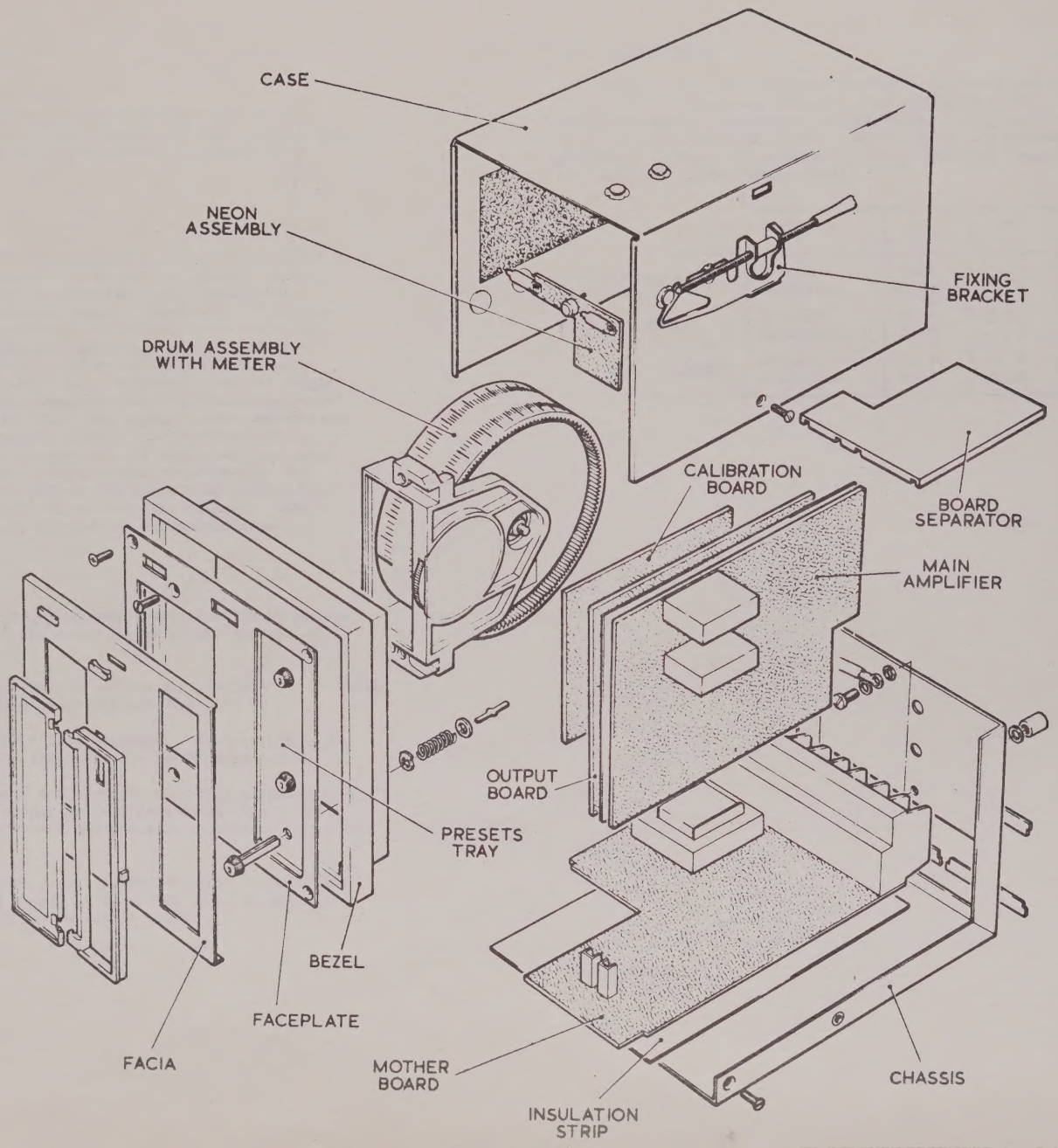
CASE
NEON ASSEMBLY
FIXING BRACKET
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BOARD SEPARATOR
MAIN AMPLIFIER
OUTPUT BOARD
PRESETS TRAY
BEZEL
FACEPLATE
FACIA
MOTHER BOARD
INSULATION STRIP
CHASSIS

MOTHER BOARD

Function

The mother board provides the necessary interconnections between the plug-in calibration, amplifier, output and alarm boards. It also carries the components necessary for generating the instrument power supplies and for driving the temperature indicator.

Circuit Description

A smooth, isolated unstabilised -28V d.c. supply is obtained across C2 from the centre-tapped transformer secondary via diodes D2, D4, D5. Full-wave rectification is provided by D2, D4 and D5 effectively isolates the -28V smoothed supply from the -24V unsmoothed supply. Diodes D1, D3 provide an unsmoothed +24V supply. A reference voltage of -8.2V is provided at T3 base by the zener diode Z1 mounted on the main amplifier board. Emitter-follower T3 uses this reference voltage to provide a stabilised -9V supply at the emitter via the emitter load resistor R10. The stabilised -4V supply is derived from the main amplifier board components Z1, T13 with mother-board resistor R8 acting as an emitter load for T13. The signal to the temperature-indicating error meter is required to remain constant as the bandwidth is altered. Connection of the error meter between the -4V supply and the wiper of the main amplifier bandwidth control P1 fulfils this requirement. The emitter followers T1, T2 are included to prevent the meter from loading P1. Resistor R6 provides base current drive to T2 so that this current is not drawn from P1. Transistors T1 and T2 are matched for Veb to minimise temperature drift and offset.

Checking

1. Insert the main amplifier board into the mother board in order to obtain the -4V and -9V supplies. Connect the mains supply to the appropriate terminals.

2. Check the +24V and -24V unsmoothed supplies with a d.c. voltmeter. If these supplies are not present check transformer TX1 and diodes D1 to D4.

3. Check the -28V smoothed supply with a d.c. voltmeter. If this supply is not present check diode D5. If the supply is low check capacitor C2.

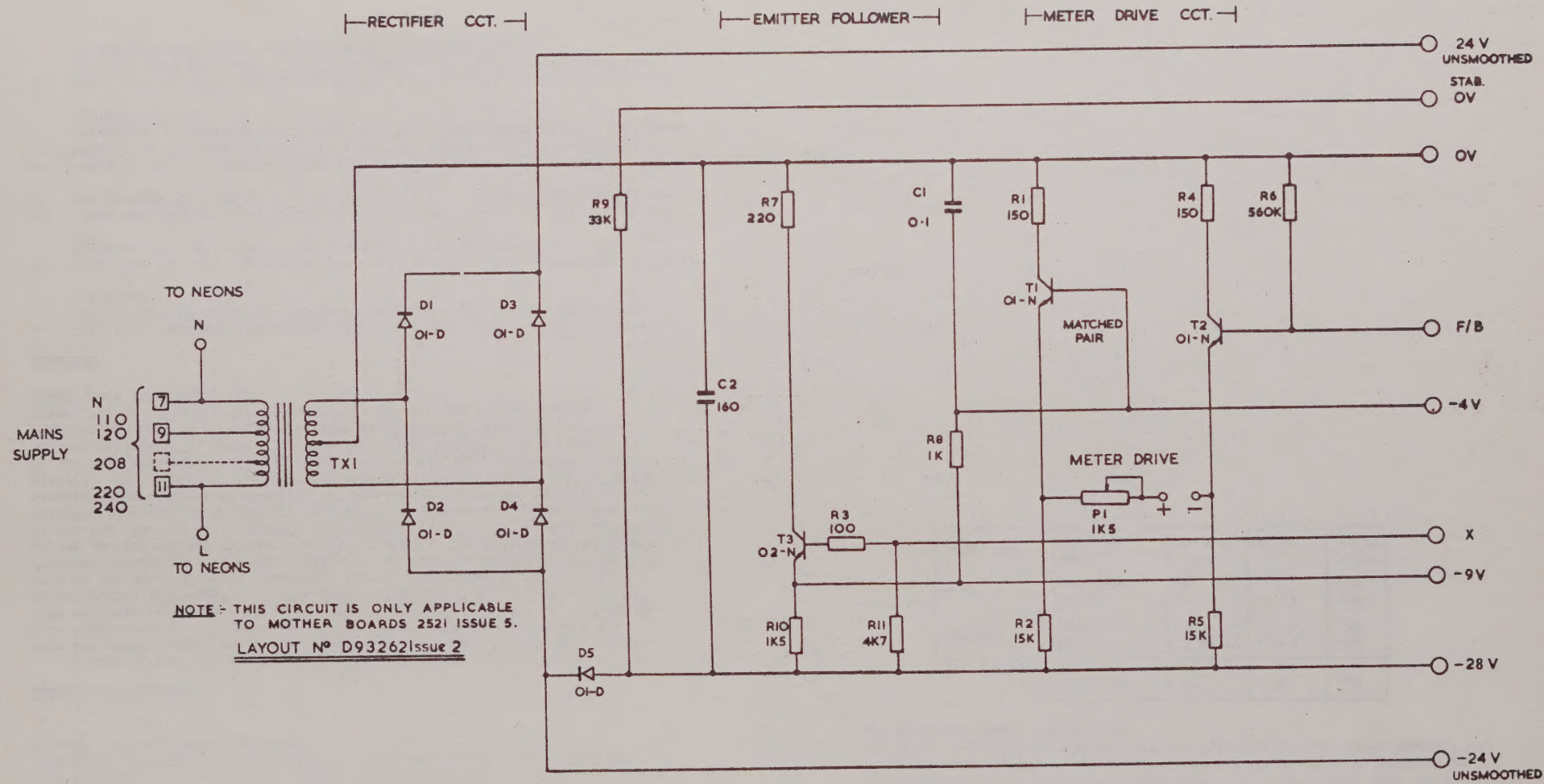
4. Check the -9V stabilised supply with a d.c. voltmeter, this normally lies between -8.6V and-9.2V. If this supply is incorrect check that a -8V reference is available at T3 base from Z1 on the main amplifier, then check operation of T3.

5. Check the -4V stabilised supply with a d.c. voltmeter, this normally lies between -3.7V and -4.1V. If this supply is incorrect check Z1 and T13 on the main amplifier board and T3 on the mother board.

D.C. Voltage table

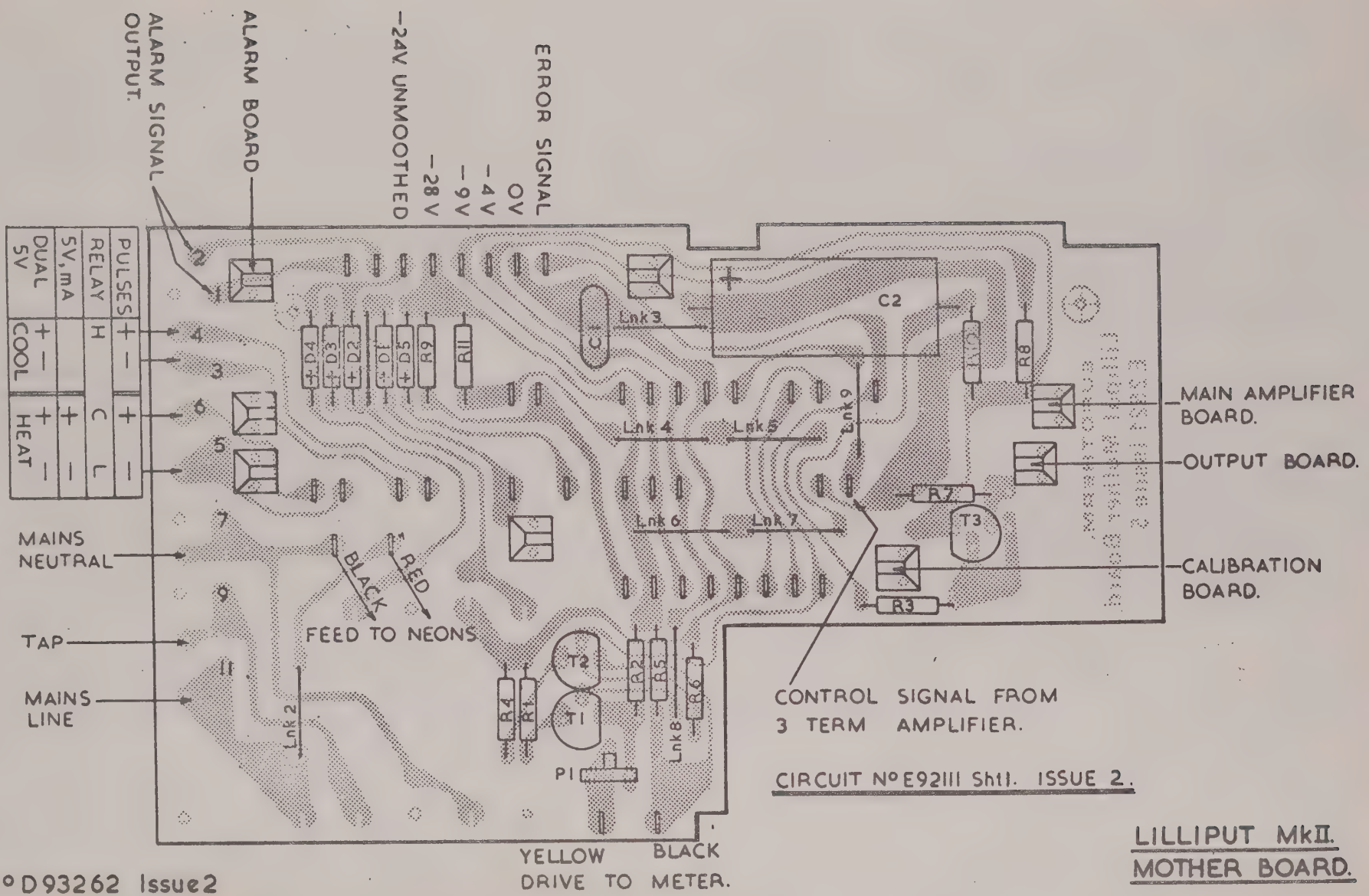
Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to 0V using a 10V d.c. voltmeter having a resistance of 20KΩ/volt. The proportional band control, P1 on the main amplifier board, must be set to its maximum fully-clockwise position. Voltages are checked with the indicator upscale (over temperature) and downscale (under temperature).

	INDICATOR	T1	T2	T3
EMITTER	UPSCALE	-4.6V	-5.5V	-9V
	DOWNSCALE	-2 V	-1 V	-9V
BASE	UPSCALE	-4 V	-7.7V	-8V
	DOWNSCALE	-4 V	-.3 V	-8V
COLLECTOR	UPSCALE	-.5 V	0 V	-1.5V
	DOWNSCALE	0 V	-0.5V	-1.2V



LILLIPUT Mk II.
MOTHER BOARD.

Drg Nº E92111 Sht 1 Issue 2



CIRCUIT Nº E92111 Sht1. ISSUE 2.

Drg Nº D93262 Issue2

LILLIPUT MkII.
MOTHER BOARD.

SLIDEWIRE THERMOCOUPLE CALIBRATION BOARD

Function

The thermocouple slidewire calibration board subtracts the thermocouple e.m.f. from the slidewire reference voltage and feeds the resultant error signal to the main amplifier inputs A and B.

Circuit Description

The required millivolt span of the controller is developed across the slidewire by the current defined by R1, P1. The thermocouple e.m.f. is subtracted from the slidewire reference voltage and the error difference is fed to the amplifier input A via R5. The filter C1, R5 rejects mains frequency series mode interference at the thermocouple input. Potentiometer P3 gives fine calibration trim at the low end of the slidewire by developing a small voltage across R6 due to current through R8. Resistor R10 is fitted for negative temperature ranges only and is normally omitted. Resistor R2 is fitted for elevated temperature ranges only and is normally replaced with a link. Resistor R9 sets the gain of the main amplifier, the required gain being dependent on the span of the controller. The negative temperature coefficient thermistor R4, in association with components R3, P2, R7, provides automatic cold junction compensation by causing the voltage across R6 to rise slightly as the ambient temperature rises. The required level of compensation is set on P2.

The resistance of thermistor R4 falls from 13KΩ at 30°C to 6KΩ at 50°C. The thermistor is removed from the circuit whilst the cold junction compensation is adjusted, the resistance change being simulated by two series resistors of value 6KΩ and 7KΩ. The resistance change from 13KΩ to 6KΩ is achieved by shorting the 7KΩ resistor. The change in cold junction e.m.f. corresponding to the 7KΩ change in resistance is injected at the input of the controller and P2 is adjusted so that the resistance change compensates for the change in cold junction e.m.f. The change in cold junction e.m.f. between 30°C and 50°C is shown in the table for the more common thermocouples.

IC	1.08mV
CA	.82mV
CC	.833mV
Pt 10%, Pt 13% Rh	.125mV

Cold Junction Compensation

The procedure for adjusting the CJC potentiometer P2 is as follows. Check the meter mechanical zero and adjust if necessary. Set P2 to its fully anticlockwise (zero compensation) position and set the proportional band to minimum. Open LK1 to remove the thermistor and insert the (6KΩ + 7KΩ) resistor chain into the sockets provided for this purpose. Inject any convenient level of millivolts and set the slidewire to give a null on the error meter. Re-check the null by placing a sensitive meter at the error amplifier output between the junction of R12, R13 and the -4V supply. Decrease the input millivolts by the amount shown in the above table. Short out the 7KΩ resistor and adjust P2 until an error meter null is again obtained. Re-check the null at the amplifier output using a sensitive meter. Remove the resistor short and return to the original level of millivolts. Re-adjust the slidewire to give a meter null if necessary and repeat the procedure until no further adjustment of the slidewire or P2 is necessary to obtain both null conditions. Remove the resistor chain, replace LK1 and calibrate the controller in the normal manner.

Meter Mechanical Zero

Place the controller on a level surface in the normal mounting position with the case removed and the mains supply disconnected. Check that the indicator aligns exactly with the set-point index and adjust if necessary by moving the spring-loaded magnet retainer.

Calibration

Check the meter mechanical zero as described above. Connect the controller to the calibrator with the correct compensating lead, being careful to observe the correct polarity. Switch on the supply and allow 5 minutes for the controller to stabilise, allowing longer if either the controller or the calibrator has been moved from warmer or cooler surroundings.

If the calibrator is a cold-junction-compensated millivolt source the calibration procedure is as follows. Turn the controller scale to maximum temperature. Read the millivolt figure equivalent to maximum temperature from the thermocouple tables and set the calibrator to this figure. Adjust P1 until the indicator also shows maximum temperature. Turn the controller scale to minimum temperature. Read the millivolt figure equivalent to minimum temperature from the thermocouple tables and set the calibrator to this figure. Adjust P3 until the indicator also shows minimum temperature. Repeat the P1 and P3 adjustments as necessary.

If the calibrator is an uncompensated potentiometer a cold-junction correction must be made when setting the maximum and minimum signals on the potentiometer. The cold junction appears at the potentiometer terminals and a thermometer is usually located adjacent to these terminals for correction purposes. Read the temperature on this thermometer and obtain the equivalent millivolts from the thermocouple tables. Read the millivolt figures equivalent to maximum and minimum controller temperatures and subtract the cold junction millivolts from each of these figures. Use the corrected figures to calibrate the controller as described above. If the minimum controller temperature is 0°C the subtraction gives a negative figure. Calibration at 0°C is achieved by reversing the polarity of the compensating lead at the potentiometer terminals and setting the potentiometer to the cold junction millivolts. Remember to reconnect the compensating lead in the correct polarity when making the maximum temperature adjustment. No correction is required for thermocouple lead resistance.

Calibration Chart

	0 to 200°C I.C.	0 to 250°C I.C.	0 to 300°C I.C.	0 to 400°C I.C.	0 to 600°C I.C.	0 to 200°C C.A.	0 to 250°C C.A.	0 to 300°C C.A.	0 to 400°C C.A.	0 to 600°C C.A.	0 to 800°C C.A.	0 to 1000°C C.A.	0 to 1200°C C.A.	0 to 1200°C Pt 10% Rh. Pt.	0 to 1600°C Pt 10% Rh. Pt.	0 to 1200°C Pt 13% Rh. Pt.	0 to 1600°C Pt 13% Rh. Pt.	
P1	1K	1K		470	470	1K	470	470	470	1K	470	470	470	1K	1K	1K	470	
R1	6K2	5K1		3K	2K2	8K2	7K5	6K2	3K9	2K4	1K8	1K6	1K4	5K6	3K9	5K1	3K6	
R9	27K	22K		12K	8K2	33K	27K	22K	18K	12K	9K1	8K2	6K8	33K	18K	18K	15K	

For scales having a minimum temperature of 0°C, R10 is omitted and R2 is replaced with a link. For other scale ranges see Drawing E2674.

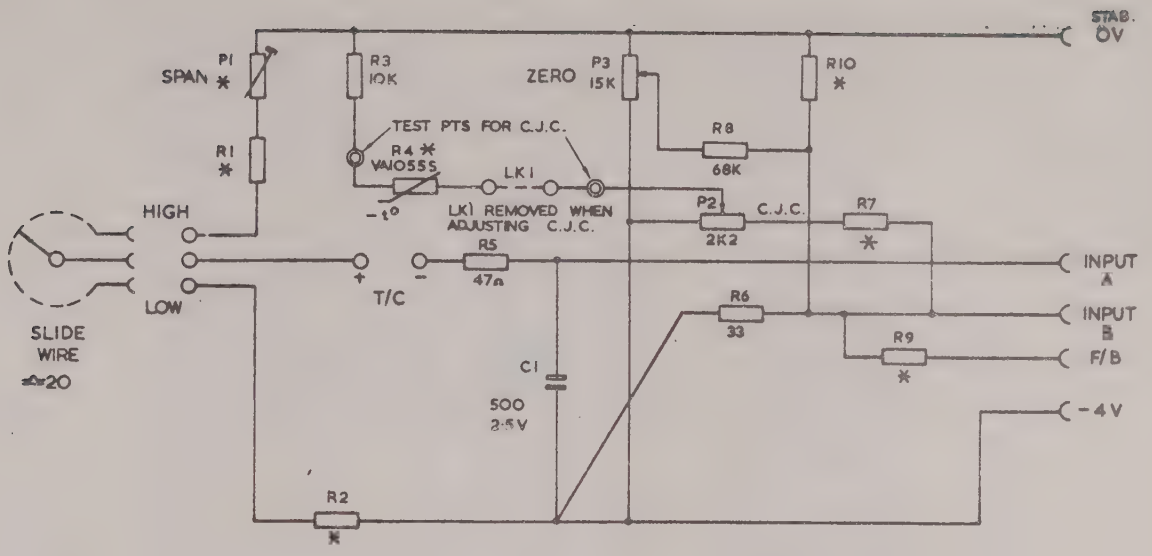
Checking

1. Check the faston connections to the slidewire and check the resistance of the slidewire with a resistance meter. This should be approximately 20 ohms.

2. Check the faston connections to the rear terminal block and check the resistance of the thermocouple. This should be less than 100 ohms.

3. Check the -4V supply to the calibration board. Note that the main amplifier board must also be connected to the mother board.

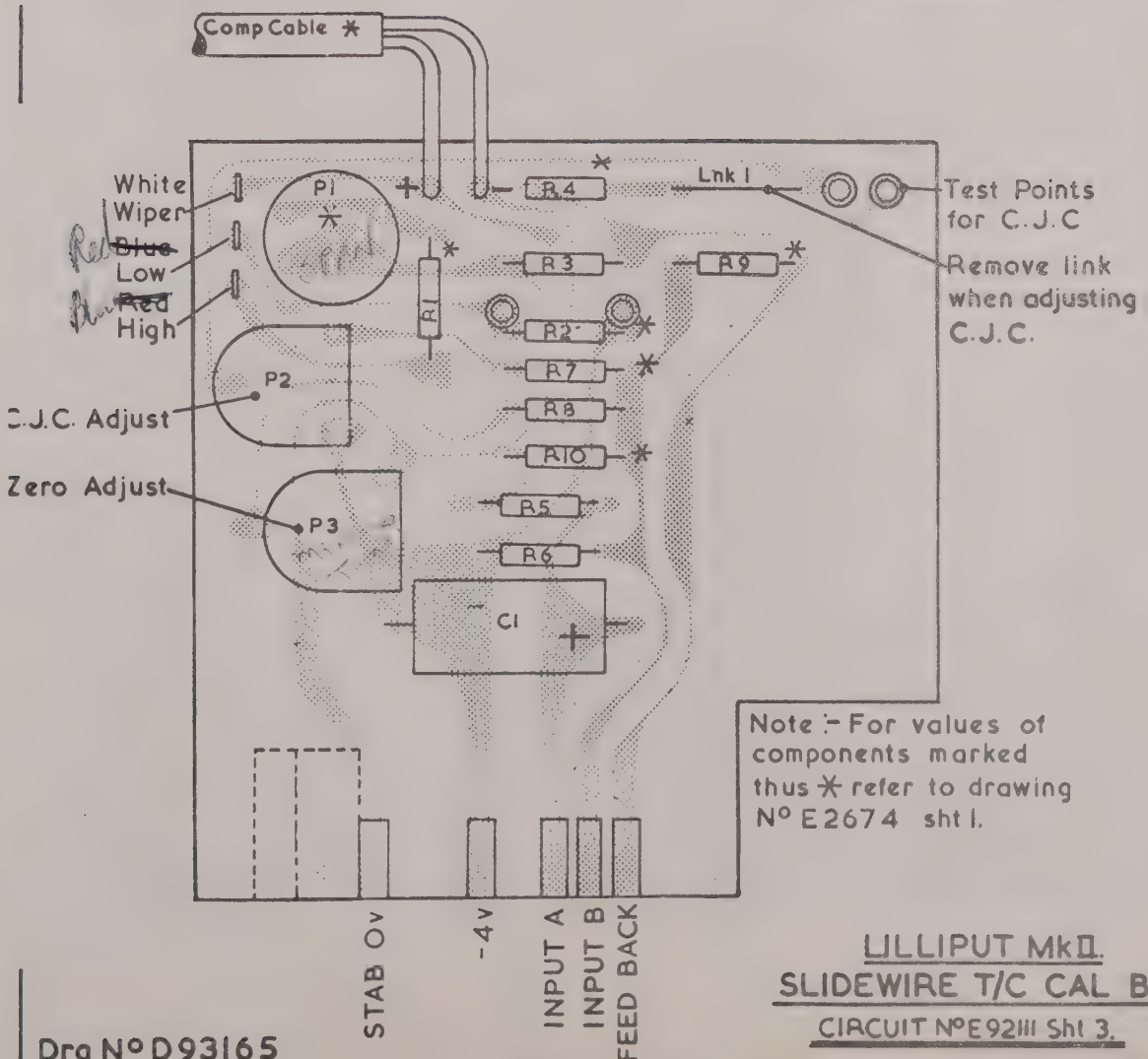
4. If the calibration board has to be replaced, adjust the cold junction compensation and the calibration as described.



COMPONENTS SHOWN THUS * VARY WITH THERMOCOUPLE AND SCALE RANGE.
REFER TO WRITE UP FOR DETAILS.

LILLIPUT Mk II.
SLIDEWIRE T/C CAL BOARD.
LAYOUT Nº D93165

Dra Nº E92111 Sht 3



LILLIPUT Mk II.
SLIDEWIRE T/C CAL B'd.
CIRCUIT Nº E92111 Sht 3.

Drg Nº D93165

Resistance Thermometer Calibration Board

Function

The platinum resistance thermometer slidewire calibration board effectively subtracts the voltage drop across the resistance thermometer from the slidewire reference voltage to produce an error signal. These voltages are fed to the main amplifier inputs A and B.

Circuit Description

The required millivolt span of the controller is developed across the slidewire by the current defined by R1, P1. The control temperature is set by tapping the reference voltage from the slidewire and this voltage is applied to input A of the main amplifier via R4. The voltage developed across the resistance thermometer by the nearly constant resistance thermometer current is applied to input B of the main amplifier via R8. The resistance thermometer voltage is thus effectively subtracted from the reference voltage.

The current flowing through the resistance thermometer is defined by R5, R6, P3. At 0°C, the thermometer has a resistance of 100 ohms and offset of the reference voltage is required for zero adjustment. This offset is obtained by means of R2, P2. Potentiometer P3 is adjusted to eliminate current flow in the V1 wire by equalising the currents in R5 and R6.

Components R4, C1 form a filter to provide mains frequency series mode pick-up rejection and C2 provides high frequency interference rejection. Resistor R3 is fitted when zero offset spans are required. Resistor R9 defines the gain of the main amplifier, the required gain being dependent on the span of the controller.

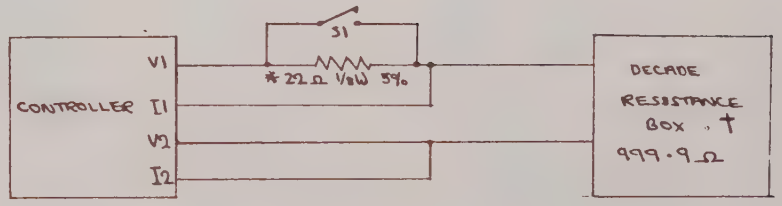
Calibration Table

100 ohm bulb @ 0°C.

SCALE	SPAN	P1 Ω	R1	R2 Ω	R3 Ω	P2 Ω	R5	R6	P3	R9	R7
0-100°C	40mV	470	1K8	82	75	100	3K9	3K3	2K	47K	18K
0-200°C	40mV	470	1K8	56	33	100	7K5	8K2	2K	56K	18K
0-400°C	40mV	470	1K8	27	18	100	15K	15K	10K	62K	18K

Calibration

The test set-up shown below is required :-



† To be set to a value equal to the thermometer resistance at each drum scale setting

* The 22Ω resistor simulates resistance in the V_1 wire

Short out the 22 ohm resistor by closing S1. Set the scale drum to 0°C and set the decade box to 100Ω. Adjust the span control P1 only, to obtain null error at 0°C. Set the scale drum and decade box to values corresponding to 85% of span and note the error offset, plus or minus X. Then adjust P1 to give an offset of

$$\pm \left(\frac{\text{Thermometer resistance at 85\% of span}}{\text{(Thermometer resistance at 85\% of span - Thermometer resistance at 0°C)}} \right) .X$$

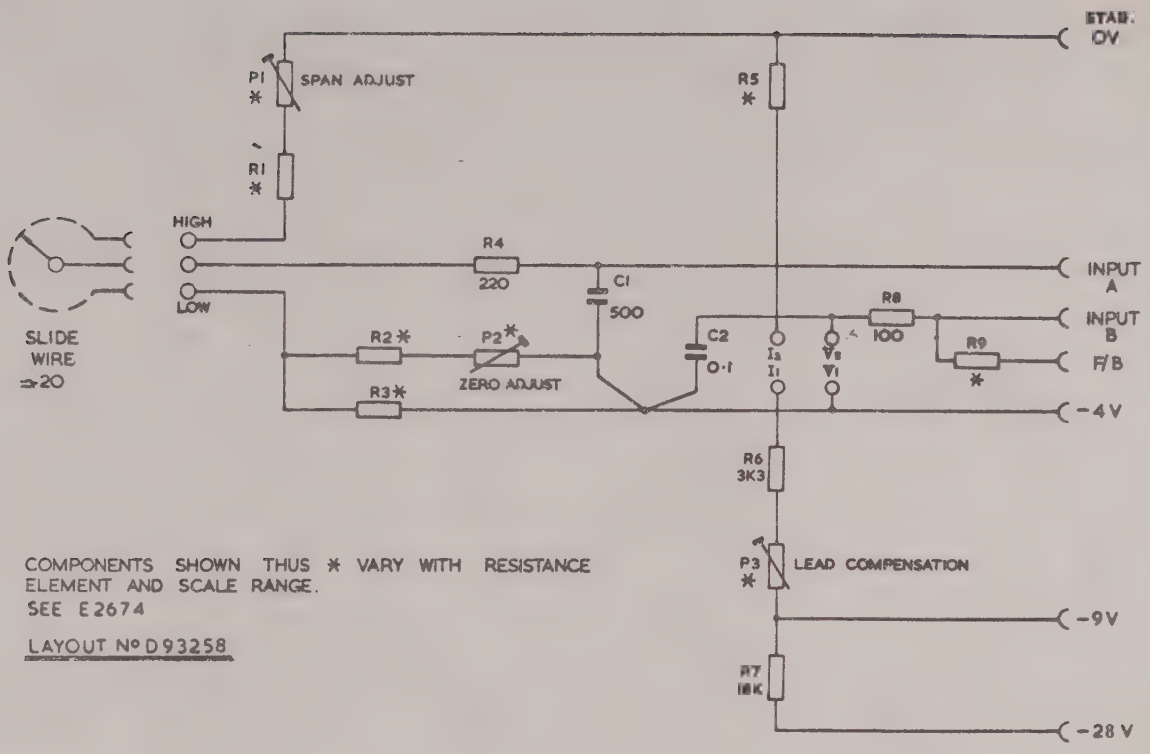
i.e. for 0 to 100°C, ± 4X; for 0 to 200°C, ± 2.5X; for 0 to 400°C, ± 1.8X

Set the scale drum and decade box to values corresponding to 0°C. Adjust the zero control P2 to obtain null error. Repeat the span and zero calibration steps until both are correct.

Set drum and decade box to values corresponding to 50% span. Open switch S1 and adjust the lead compensation control P3 to give no change in meter indication as S1 is closed and opened. Proportional band, meter follow and limit settings (if applicable) should be made at approximately 80% span for resistance thermometer units.

Note

Thermometer resistance at 50°C = 120 Ω
Thermometer resistance at 100°C = 139 Ω
Thermometer resistance at 200°C = 176 Ω

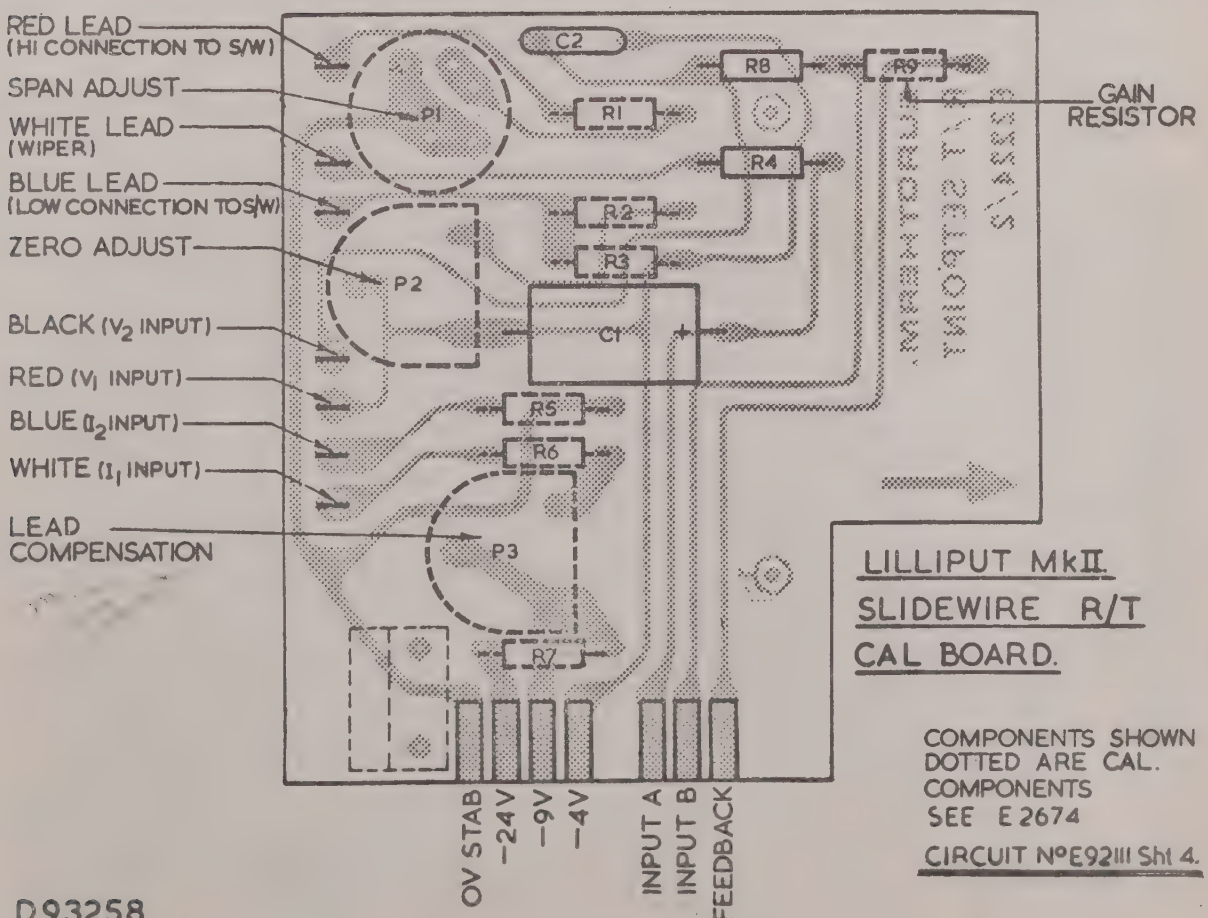


COMPONENTS SHOWN THUS * VARY WITH RESISTANCE ELEMENT AND SCALE RANGE.
SEE E2674

LAYOUT Nº D93258

LILLIPUT MkII.
SLIDEWIRE R/T CAL B'd

Drg Nº E92111 Sht 4



LILLIPUT MkII.
SLIDEWIRE R/T
CAL BOARD.

COMPONENTS SHOWN DOTTED ARE CAL. COMPONENTS
SEE E2674

CIRCUIT Nº E92111 Sht 4.

D93258

Thermocouple Digital Calibration Board

Function

The thermocouple digital calibration board subtracts the thermocouple e.m.f. from the digitally set, linearised reference voltage and feeds the resultant error signal to the main amplifier input.

Circuit Description

The reference voltage is obtained by digital switches S1 to S3 (S1 to S4 for four digits) tapping three (four) voltages from the resistor chain R1 to R10 (see drawings C92111, sheets 10, 11, 12). These tapped voltages are scaled by resistors R11, R12, R13 (and R14) and added in resistor R1 which is connected across the input of the amplifier formed by transistors T1 to T3.

Transistors T1 to T3 and associated components form a buffer amplifier to prevent loading of the reference circuit. After buffering, the amplified reference voltage is applied to a series of linearising circuits formed by transistors T4 to T9 and associated components. The linearising circuits modify the reference input from the digital switches to produce a characteristic which closely matches the particular thermocouple characteristic. This matching is obtained by applying cut (slope decrease) or lift (slope increase) to the low and high ends of the reference characteristic.

Transistors T4, T5 form a low cut circuit which decreases the slope of the reference characteristic at low values of reference voltage below a value defined by the bias on T5 base. Transistors T6, T7 form a second low cut circuit which modifies the slope of the reference characteristic for signal levels below the value defined by the bias on T7 base. Diodes D1, D2 and associated components form a gating circuit which provides low signal lift. Transistors T8, T9 provide either high signal lift or cut depending on the link configuration. The net current flowing in the linearising network is fed to the R32, R33 parallel combination to produce the required reference.

Automatic cold junction temperature compensation is provided by the negative temperature coefficient thermistor R35 in association with components R34, P3, R37, R38. The voltage across R38 is caused to rise slightly as the ambient temperature rises. The required level of compensation is set on P3. Components R36, C4 form a series mode interference filter which rejects mains frequency pick-up at the thermocouple input.

Span adjustment is provided by P1 which defines the current flowing in the digital switch resistor chain R1 to R10. Zero adjustment is provided by P2 which allows a current bleed through R32, R33 via R30 to compensate for offset which may exist at the output of the linearising network. Resistor R40 defines the gain of the main amplifier, the required gain being dependent on the span of the controller. Capacitors C1, C2 and C3 provide stabilisation of the amplifier and linearising circuits.

Cold Junction Compensation

The resistance of thermistor R35 falls from 13KΩ at 30°C to 6KΩ at 50°C. The thermistor is removed from the circuit whilst the cold junction compensation is adjusted, the resistance change being simulated by two series resistors of value 6KΩ and 7KΩ. The resistance change from 13KΩ to 6KΩ is achieved by shorting the 7KΩ resistor. The change in cold junction e.m.f. corresponding to the 7KΩ change in resistance is injected at the input of the controller and P3 is adjusted so that the resistance change compensates for the change in cold junction e.m.f. The change in cold junction e.m.f. between 30°C and 50°C is shown in the table for the more common thermocouples.

IC	1.08mV
CA	.82mV
CC	.833mV
Pt 10%, Pt 13% Rh	.125mV

The procedure for adjusting the CJC potentiometer P3 is as follows. Check the meter mechanical zero and adjust if necessary. Set P3 to its fully anticlockwise (zero compensation) position and set the proportional band to minimum. Open LK1 to remove the thermistor and insert the (6KΩ + 7KΩ) resistor chain into the sockets provided for this purpose. Inject any convenient level of millivolts and set the slidewire to give a null on the error meter. Re-check the null by placing a sensitive meter at the error amplifier output between the junction of R12, R13 and the -4V supply. Decrease the input millivolts by the amount shown in the above table. Short out the 7KΩ resistor and adjust P3 until an error meter null is again obtained. Re-check the null at the amplifier output using a sensitive meter. Remove the resistor short and return to the original level of millivolts. Re-adjust the digit switch to give a meter null if necessary and repeat the procedure until no further adjustment of the digit switch or P3 is necessary to obtain both null conditions. Remove the resistor chain, replace LK1 and calibrate the controller in the normal manner.

Calibration

Adjust the meter mechanical zero as follows:-

Place the controller on a level surface in the normal mounting position with the case removed and the mains supply disconnected. Check that the error meter indicator aligns exactly with the zero mark and adjust if necessary by turning the nylon screw.

Connect the controller to the calibrator with the correct compensating lead, being careful to observe the correct polarity. Switch on the supply and allow 5 minutes for the controller to stabilise, allowing longer if either the controller or the calibrator has been moved from warmer or cooler surroundings.

If the calibrator is a cold-junction-compensated millivolt source the calibration procedure is as follows. Set the digit switch to maximum temperature. Read the millivolt figure equivalent to maximum temperature from the thermocouple tables and set the calibrator to this figure. Adjust P1 until a null indication is obtained on the error meter. Set the digit switch to a temperature near to zero. Read the millivolt figure equivalent to this low temperature from the thermocouple tables and set the calibrator to this figure. Adjust P2 until a null indication is obtained on the error meter. Repeat the P1 and P2 adjustments as necessary.

If the calibrator is an uncompensated potentiometer a cold-junction correction must be made when setting the maximum and minimum signals on the potentiometer. The cold junction appears at the potentiometer terminals and a thermometer is usually located adjacent to these terminals for correction purposes. Read the temperature on this thermometer and obtain the equivalent millivolts from the thermocouple tables. Read the millivolt figures equivalent to maximum and minimum controller temperatures and subtract the cold junction millivolts from each of these figures. Use the corrected figures to calibrate the controller as described above. If the minimum controller temperature is $0^{o}C$ the subtraction gives a negative figure. Calibration at $0^{o}C$ is achieved by reversing the polarity of the compensating lead at the potentiometer terminals and setting the potentiometer to the cold junction millivolts. Remember to reconnect the compensating lead in the correct polarity when making the maximum temperature adjustment. No correction is required for thermocouple lead resistance.

Checking

1. Check all faston connections to the calibration board and check the resistance of the thermocouple. This should be less than 100 ohms.

2. Check the -4V supply to the calibration board. Note that the main amplifier board must also be connected to the mother board.

3. Disconnect the output of the digital switch assembly to the calibration board and connect a d.c. voltmeter between -4V supply and the switch output. Set the switches to zero and check that the output voltage is zero.

4. Increase the digit switch setting slowly up to the maximum value and check that equal increments of voltage occur for each decade. The switch resistor chain tappings provide .4V increments between 0 and +3.6V measured directly on the switch wipers.

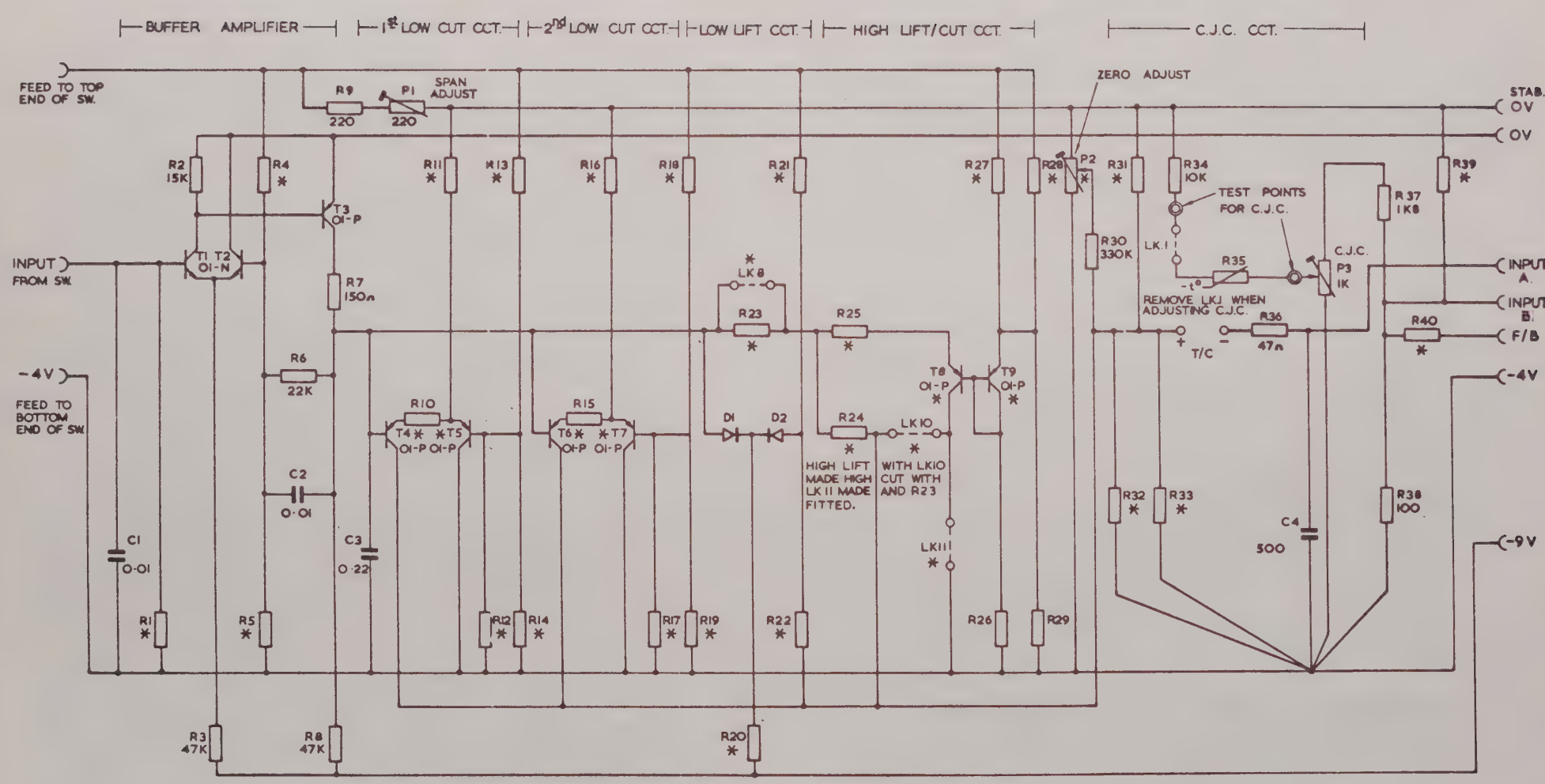
   NOTE:- In cases where the first digit is stopped at 1, e.g. $1200^{o}C$, the 1 is normally taken to a higher tap on the resistor chain. This ensures that adequate signal is always available for the reference circuit without recourse to increased gain in the calibration board buffer amplifier. Therefore, the maximum output from the digit switch will vary with different spans. The amplifier gain is adjusted such that the amplifier output at the junction of R7, R8 is 3.24V for all spans.

5. If the calibration board has to be replaced, adjust the cold junction compensation and the calibration as described.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to 0V using a d.c. voltmeter having a resistance of 20K /Volt.

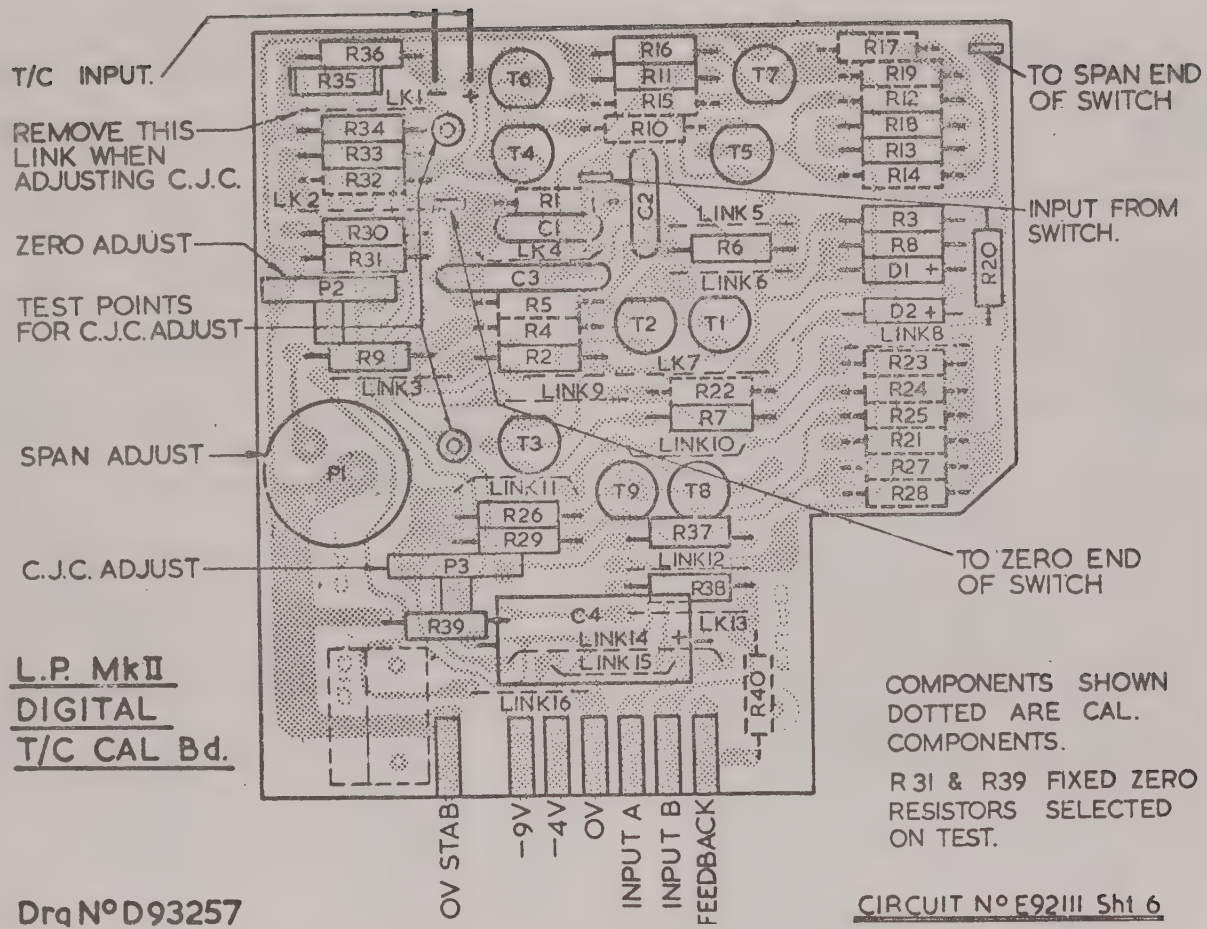
	DIGITAL SETTING	T1	T2	T3	T4	T5	T6	T7	T8	T9
EMITTER	0	-4.6	-4.6	0	-3.5	-3.2	+3.5	-2.5	-3.3	-2 V
	MAX	-1.3	-1.3	0	-2.8	-3.2	-2	-2.5	-2	-2 V
BASE	0	-3.5	-4.1	-0.6	-4	-3.6	-0.6	-2.8	-2	-2 V
	MAX	-0.6	-0.7	-0.6	-0.2	-3.6	-0.2	-2.8	-2	-2 V
COLLECTOR	0	-0.6	0	-4	-4	-4	-4	-4	-4	-2 V
	MAX	-0.6	0	-ve	-4	-4	-4	-4	-4	-2V



COMPONENTS SHOWN THUS * WILL BE OMITTED OR INCLUDED, & / OR THEIR VALUES WILL CHANGE, ACCORDING TO THE THERMOCOUPLE & SWITCH RANGE.
REFER TO WRITE UP FOR DETAILS.

LILLIPUT MkII.
DIGITAL T/C CAL BOARD.
LAYOUT Nº D93257

Drg Nº E92111 Sht 6



L.P. MkII DIGITAL T/C CAL Bd.

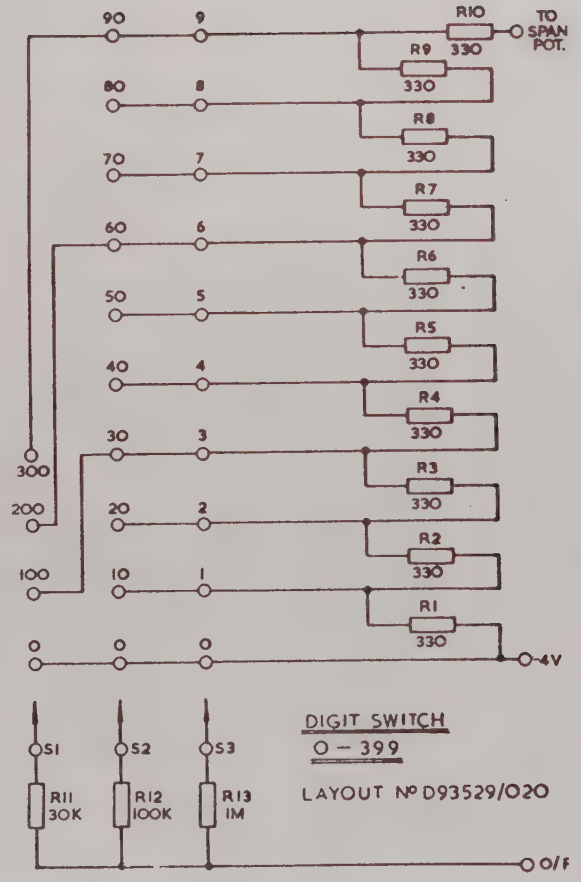
COMPONENTS SHOWN DOTTED ARE CAL. COMPONENTS.

R 31 & R39 FIXED ZERO RESISTORS SELECTED ON TEST.

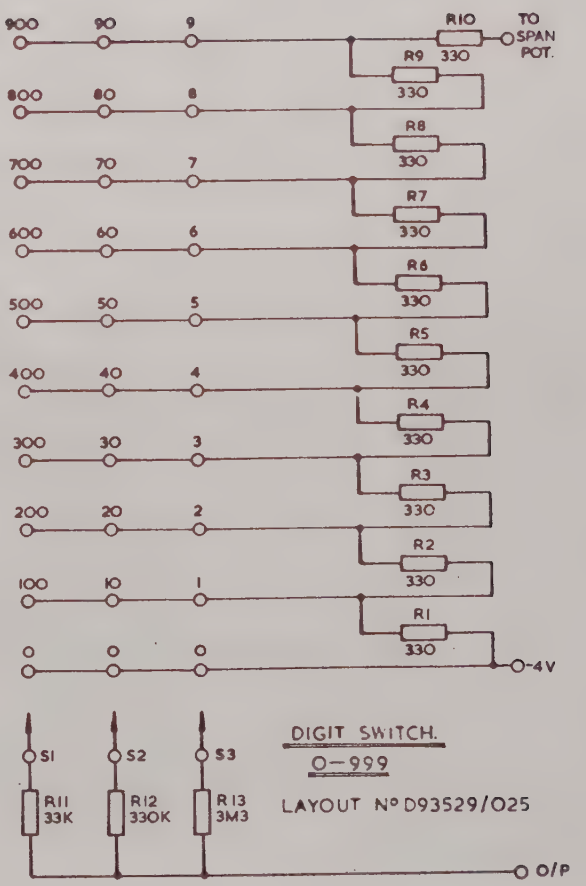
Drg No D93257

CIRCUIT No E92111 Sht 6

Digital T/C Cal Board



Drg Nº C92111 Sht 10



Drg Nº C92111 Sht 11.

REAR VIEW
SHOWING LINKING METHOD

FRONT VIEW
SHOWING SWITCH
IN MAX. POSITION

CIRCUIT Nº E92111 Sht 11

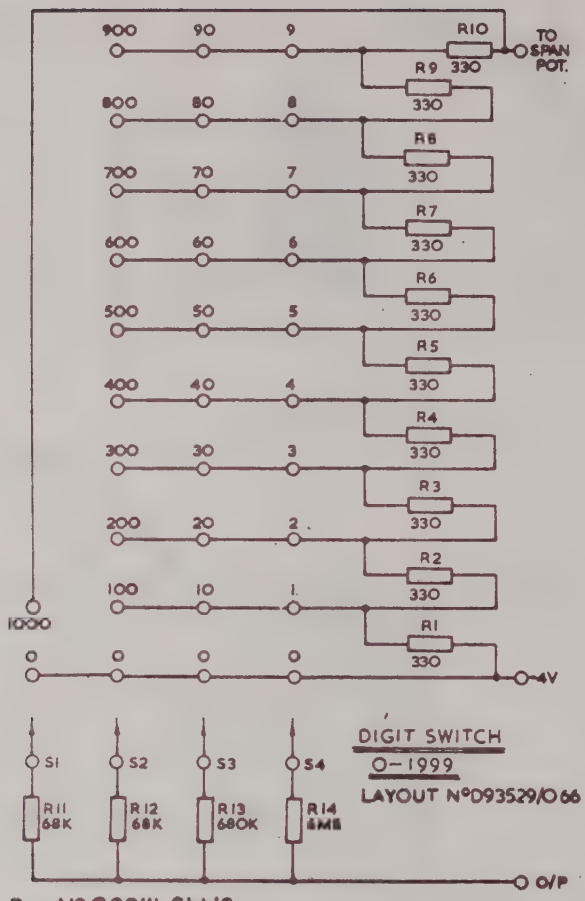
Drg NºD93529/025

REAR VIEW
SHOWING LINKING METHOD

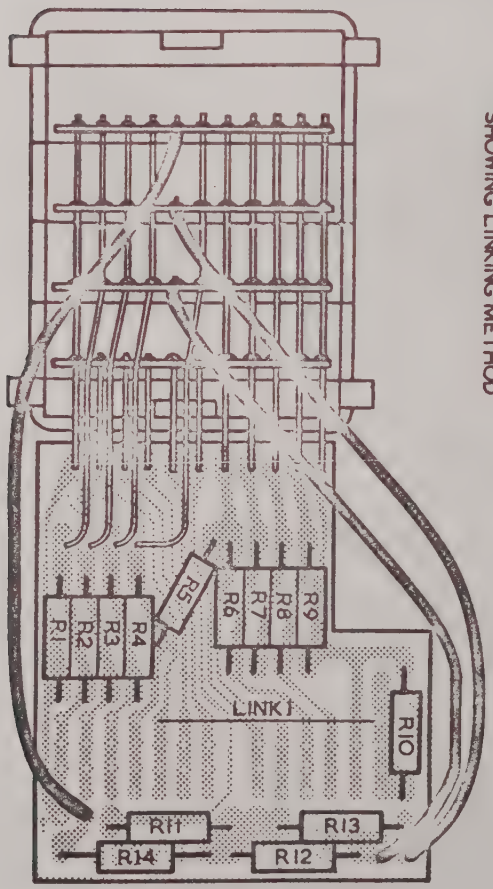
FRONT VIEW
SHOWING SWITCH
IN MAX. POSITION

CIRCUIT Nº E92111 Sht 10

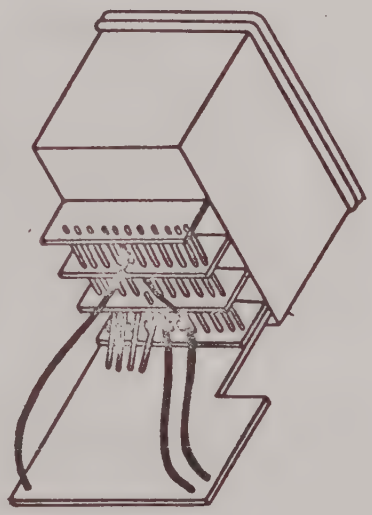
Drg NºD93529/020



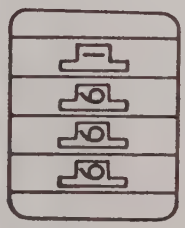
Drg NºC92111 Sht 12



REAR VIEW SHOWING LINKING METHOD



FRONT VIEW SHOWING SWITCH IN MAX. POSITION



Drg NºD93529/066

CIRCUIT NºE92111 Sht 12

DRG. No E 2674/

THIRD ANGL

GROUP 3 CODE (INPUT)	GROUP 4 CODE (SPAN)	P.C.B. ASSY PART No.	R1 1/2W 2% M.O. or 1/2W 2% M.F.	R2. S.O.T NOMINAL VALUES SHOWN FOR GUIDANCE ONLY.	R4	R7 1/8W 5% CARBON	R9 1/8W 5% CARBON	R10. S.O.T. NOMINAL VALUE SHOWN FOR GUIDANCE ONLY.	P1 PLESSEY MPD W/N	THERMOCOUPLE COMPENSATION CABLE STANDARD
04 Cu/Con. Bs	017 0-200°C	2674/04017	7K5 RSY 752	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	27K RSS 273		1K PTP 102	RED C3222
04	096 0-800°C	2674/04096	4K7 RSY 472	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	18K RSS 183		1K PTP 102	RED C3222
04	020 0-400°C	2674/04020	3K RSY 302	LINK LPB 012	VA 10555 VA 10555	1K2 RSS 122	12K RSS 123		1K PTP 102	RED C3222
98 LINEAR	010 -15+15mv.	2674/98010	2K2 RSY 222	LINK LPB 012	15K RSY 153	1K2 RSS 122	8K2 RSS 822	12K RSS 123	470 PTP 471	Cu WIRE D3616/25 D3616/26
98	011 -6+6mv.	2674/98011	5K6 RSY 562	LINK LPB 012	15K RSY 153	1K2 RSS 122	22K RSS 223	27K RSS 273	1K PTP 102	Cu WIRE D3616/25 D3616/26
98	012 -3+3m.v.	2674/98012	10K RSY 103	LINK LPB 012	15K RSY 153	1K2 RSS 122	47K RSS 473	68K RSS 683	5K PTP 502	Cu WIRE D3616/25 D3616/26
06 Pt/Pt 10%Rh	026 0-1200°C	2674/06026	5K6 RSY 562	LINK LPB 012	VA 10555 THM 055	8K2 RSS 822	22K RSS 223		1K PTP 102	GREEN C3223
06	028 0-1600°C	2674/06028	3K9 RSY 392	LINK LPB 012	VA 10555 THM 055	8K2 RSS 822	15K RSS 153		1K PTP 102	GREEN C3223
06	136 32-2900°C	2674/06136	3K9 RSY 392	LINK LPB 012	VA 10555 THM 055	8K2 RSS 822	15K RSS 153		1K PTP 102	GREEN C3223
05 Pt/Pt 13%R.h	026 0-1200°C	2674/05026	5K1 RSY 512	LINK LPB 012	VA 10555 THM 055	8K2 RSS 822	22K RSS 223		1K PTP 102	GREEN C3223
05	028 0-1600°C	2674/05028	3K6 RSY 362	LINK LPB 012	VA 10555 THM 055	8K2 RSS 822	15K RSS 153		1K PTP 102	GREEN C3223
05	136 32-2900°F	2674/05136	3K6 RSY 362	LINK LPB 012	VA 10555 THM 055	8K2 RSS 822	15K RSS 153		1K PTP 102	GREEN C3223
05	095 350-850°C	2674/05095	12K RSY 123	10 RSS 101	VA 10555 THM 055	8K2 RSS 822	47K RSS 473		2K PTP 202	GREEN C3223
05	042 800-1400°C	2674/05042	8K2 RSY 822	19 RSS 191	VA 10555 THM 055	8K2 RSS 822	33K RSS 333		2K PTP 202	GREEN C3223
07 Pt 5% Rh/Pt 20% Rh	029 0-1800°C	2674/07029	5K6 RSY 562	LINK LPB 012	15K RSY 153	1K2 RSS 122	22K RSS 223		1K PTP 102	Cu WIRE D3616/25 D3616/26
08 Pt 6% Rh/Pt 30% Rh	029 0-1800°C	2674/08029	5K1 RSY 512	LINK LPB 012	15K RSY 153	1K2 RSS 122	18K RSS 183		1K PTP 102	Cu WIRE D3616/25 D3616/26
* 18 IR 40% Rh/IR	044 1000-1800°C	2674/18044	15K RSY 153	25 RSS 251	VA 10555 THM 055	8K2 RSS 8K2	68K RSS 683		5K PTP 502	Cu WIRE D 3616/25 D 3616/26

FOR THESE ASSEMBLIES USE BASIC ASSY. E2219

* SPECIAL CARE IS REQUIRED WITH THE APPLICATION OF 2674/18044 AS SPAN IS < 5m.v.

DRAWN	S.H.	TITLE P.C.B. ASSY. LILLIPUT MK I T/C CALIBRATION & L.C. CAL. COMPONENTS).
CHECKED	D.G.S.	
DESIGN APPROVAL		
PRODUCTION APPROVAL		DRG. No. E 2674/ Sht 2

GROUP 3 CODE (INPUT)	GROUP 4 CODE (SPAN)	P.C.B. ASSY PART NO.	R1 ½W. 2% M.O. ½W. 2% M.F.	R2 S.O.T. NOMINAL VALUES SHOWN FOR GUIDANCE ONLY	R4	R7 ⅛W. 5% CARBON	R9 ⅛W. 5% CARBON	R10. S.O.T. NOMINAL VALUES SHOWN FOR GUIDANCE ONLY.	P1 PLESSEY MPD. W/W	THERMOCOUPLE COMPENSATION CABLE STANDARD.
03 C/A BS. DIN ASA	017 0-200°C	2674/03017	8K2 RSY 822	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	33K RSS 333		2K PTP 202	RED C3222
03	018 0-250°C	2674/03018	6K8 RSY 682	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	27K RSS 273		1K PTP 102	RED C3222
03	096 0-300°C	2674/03096	5K6 RSY 562	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	22K RSS 223		1K PTP 102	RED C3222
03	020 0-400°C	2674/03020	3K9 RSY 392	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	15K RSS 153		1K PTP 102	RED C3222
03	023 0-600°C	2674/03023	2K7 RSY 272	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	10K RSS 103		470 PTP 471	RED C3222
03	024 0-800°C	2674/03024	2K RSY 202	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	8K2 RSS 822		470 PTP 471	RED C3222
03	025 0-1000°C	2674/03025	1K6 RSY 162	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	6K2 RSS 622		470 PTP 471	RED C3222
03	026 0-1200°C	2674/03026	1K3 RSY 132	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	5K6 RSS 562		470 PTP 471	RED C3222
03	090 -200-+200°C	2674/03090	4K7 RSY 472	LINK LPB 012	VA10555 THM 055	1K2 RSS 122	18K RSS 183	39K RSS 393	1K PTP 102	RED C3222
03	068 -100+400°C	2674/03068	3K3 RSY 332	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	12K RSS 123	120K RSS 124	1K PTP 102	RED C3222
03	097 300-700°C	2674/03097	3K9 RSY 392	14 RSS 140	VA 10555 THM 055	1K2 RSS 122	15K RSS 153		1K PTP 102	RED C3222
03	116 32-400°F	2674/03116	8K2 RSY 822	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	33K RSS 333		2K PTP 202	RED C3222
03	119 32-800°F	2674/03119	3K9 RSY 392	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	15K RSS 153		1K PTP 102	RED C3222
03	124 32-1200°F	2674/03124	2K4 RSY 242	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	10K RSS 103		470 PTP 471	RED C3222
03	127 32-1650°F	2674/03127	1K8 RSY 182	LINK LPB 012	VA 10555 THM 066	1K2 RSS 122	6K8 RSS 682		470 PTP 471	RED C3222
03	132 32-2200°F	2674/03132	1K3 RSY 132	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	5K6 RSS 562		470 PTP 471	RED C3222
* 03	092 -15-80°F	2674/03092	3K3 RSY 332	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	120K RSS 124	390K RSS 394	1K PTP 102	RED C3222
01 I/C. BS. DIN ASA	017 0-200°C	2674/01017	6K2 RSY 622	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	27K RSS 273		1K PTP 102	BLACK C3221
01	018 0-250°C	2674/01018	5K1 RSY 512	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	18K RSS 183		1K PTP 102	BLACK C3221
01	096 0-300°C	2674/01096	4K3 RSY 432	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	16K RSS 163		1K PTP 102	BLACK C3221
01	020 0-400°C	2674/01020	3K RSY 302	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	12K RSS 123		1K PTP 102	BLACK C3221
01	023 0-600°C	2674/01023	2K RSY 202	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	8K2 RSS 822		470 PTP 471	BLACK C3221
01	008 -40-+80°C	2674/01008	10K RSY 103	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	43K RSS 433	180K RSS 184	5K PTP 502	BLACK C3221
01	116 32-400°F	2674/01116	6K2 RSY 622	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	22K RSS 223		2K PTP 202	BLACK C3221
01	119 32-800°F	2674/01119	2K7 RSY 272	LINK LPB 012	VA 10555 THM 055	1K2 RSS 122	12K RSS 123		1K PTP 102	BLACK C3221

TITLE P.C.B ASSY.
LILLIPUT MK II. T/C CALIBRATION BD. (CAL COMPONENTS)

DRG No. F 2674/ SH 1

MAIN AMPLIFIER BOARD

Function

The main amplifier board converts a microvolt level error signal from the calibration board into a 0 to 5 volt signal suitable for driving the output stage. The output signal varies between the -4V and -9V levels, corresponding respectively to minimum and maximum output from the controller.

Circuit Description

The board consists of three main sections, an error amplifier, a three term amplifier and a stabilised power supply. The error amplifier is a temperature stabilised high-gain d.c. amplifier with a gain control in the feedback network which allows the gain, and hence the proportional bandwidth, to be varied over a 5:1 range. The error amplifier drives the three term amplifier. The three term amplifier introduces integral and derivative action into the control loop to enable accurate control at the desired temperature with no offset. The proportional bandwidth of the controller is defined as the change in input signal required to produce a change in output signal from zero to 100%. The controller bandwidth thus corresponds to an output signal change of 5 volts at the three term amplifier output. The three term amplifier has a gain of 5 for the standard model with a 2% to 10% bandwidth. The controller bandwidth thus corresponds to an error amplifier output of 1 volt. The minimum gain of the error amplifier is set to produce an output of 1 volt when an error signal of 10% of span is applied at the input. Alternative models have a proportional bandwidth variable 1% to 5% of span or 5% to 25%, achieved respectively by increasing the three term amplifier gain to 10 or decreasing the three term amplifier gain to 2. A desaturation network placed across the three term amplifier prevents amplifier saturation and enables derivative action to take effect some 40% of span away from the set-point, thereby minimising overshoot and reducing settling time from warm-up. The output control signal is fed to the output board via a maximum power control. The power supply section provides a temperature stabilised -4V supply for the amplifier circuit and calibration board.

Error amplifier

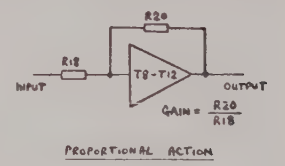
Transistors T1 to T5 and associated components form a high-gain low-drift d.c. amplifier with overall positive gain from T1 base to T5 collector. Input transistors T1, T2 are a matched pair connected differentially and surrounded by a heat sink to give very low temperature drift. Potentiometer P2 is included to balance out any difference in the resistance values of R5, R6 and set up the amplifier to give a -4V output with no input signal applied. The differential signal at the collectors of T1, T2 is further amplified by the differentially connected transistors T3, T4 and a single-ended output is provided at the collector of T5. The overall gain of the amplifier is set by providing negative feedback from T5 collector to T2 base via P1, R3 and calibration board resistors R6, R9. Potentiometer P1 is included in the feedback network to vary the proportional bandwidth over a 5:1 range by varying the gain of the amplifier. Different proportional band ranges of 1% to 5% of span, 2% to 10% of span or 5% to 25% of span are achieved by fixing the three term amplifier gain at 10, 5 or 2 respectively. The bandwidth of the controller thus corresponds to an error amplifier output of 0.5 volt on the model with a 1% to 5% bandwidth, 1 volt on the model with a 2% to 10% bandwidth, or 2.5 volts on the model with a 5% to 25% bandwidth. With the bandwidth potentiometer P1 set to its maximum position, the gain of the error amplifier is set to give an output signal of 1 volt, with reference to the -4V supply, when an input error signal of 10% span is applied to T1 base. When P1 is set to its maximum position the error amplifier gain is defined by (R9 + R6)/R6, these resistors being situated on the calibration board. The error amplifier output is measured at the junction of R12, R13. Diode D1 limits the amplifier output to approximately -10V. Network R8, C4 provides 50c/s rejection by reducing the a.c. gain of the error amplifier, enabling the thermocouple to be connected to mains potential if necessary. Capacitors C4a and C4b are connected in series in opposite polarity to accommodate voltages of either polarity, with reference to -4V, at the amplifier output. Network C3, R7 provides amplifier stabilisation and capacitors C1, C2, C5 provide interference rejection.

Three term amplifier

The three term amplifier T8 to T12 has a high input impedance FET transistor T8 as the input stage to make it suitable for use with the high value resistors R18, R20 required for the derivative and integral time constants. The amplifier has overall negative gain from T8 base to T12 emitter, the gain being defined approximately by the ratio R20/R18 and set to a value 10, 5 or 2 respectively for bandwidth ranges of 1% to 5%, 2% to 10% or 5% to 25%. A -4V input to T8 from the error amplifier results in a potential of approximately 1 volt across R22 due to the current through T8. This voltage is balanced out at T10 base by potentiometer P6 to set up the correct bias condition of -4V at T12 emitter when a -4V input is applied to T8 base. Capacitors C6 and C8 provide derivative and integral action respectively and capacitors C9, C10 provide interference rejection.

Proportional action

Proportional-only action can be achieved by opening link d1-d2 to remove derivative action and making link I1 - I2 to remove integral action. The auto-manual switch SW1 must be closed, or replaced with link, in order to give closed-loop temperature control. In this condition T12 acts as an emitter follower and the output signal at T12 emitter follows the signal at the junction of R27, R28. Negative feedback is applied via R20 and the gain of the three term amplifier is defined by R20/R18. The three term amplifier has a gain of 5 for controllers having a 2% to 10% bandwidth. A 1 volt input change from -4V to -3V, corresponding to a temperature change from set point to one bandwidth below set-point, thus produces a 5 volt output change from -4V to -9V and causes the output power to increase from zero to 100%. For controllers having a 1% to 5% bandwidth the three term amplifier has a gain of 10; an input change from -4V to -3.5V producing an output change from -4V to -9V. For controllers having a 5% to 25% bandwidth the three term amplifier has a gain of 2; an input change from -4V to -1.5V producing an output change from -4V to -9V. The output voltage at T12 emitter is prevented from becoming more negative than the collector voltage by emitter-follower action. Potentiometer P4 thus acts as a maximum power limit by restricting the negative excursion at T12 emitter. Diode D4 protects T12 from excessive reverse voltage when P4 is set to its minimum position. When the auto-manual switch is open T12 conducts due to base current through R30 and the emitter voltage closely follows the collector voltage. Potentiometer P4 thus acts as an output power control.

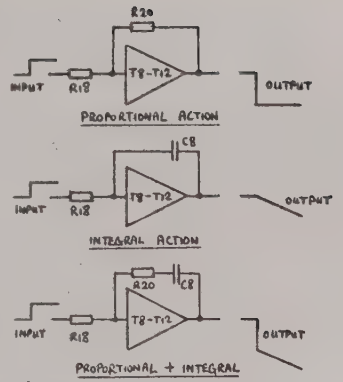


PROPORTIONAL ACTION

Integral action

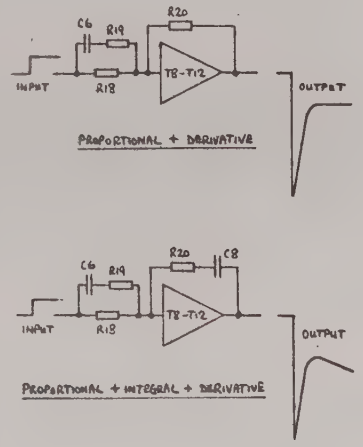
Integral action is achieved by placing capacitor C8 in series with the feedback resistor R20. The base of T8 is held at -4V by normal amplifier action and the

current through R21 is negligible due to the very high input impedance of FET transistor T8. When the error amplifier output is positive with reference to -4V, corresponding to under-temperature, a current flows through R18 due to the potential difference across R18. The three term amplifier output falls negative with reference to -4V such that all of the input current in R18 flows through R20. The negative fall at the amplifier output causes the output power to increase in proportion to the error. The input current through R18 and R20 causes capacitor C8 to charge in a direction which produces a further negative ramp at the amplifier output, the amplifier output automatically adjusting to balance the currents in R18 and R20. The negative ramp at the amplifier output causes a further gradual increase in output power. As the output power increases the temperature rises and the input signal reduces. When the load temperature achieves the desired temperature the input signal is removed and the capacitor ceases to charge. In practice C8 will always acquire just sufficient charge to enable the required output power to be maintained with a -4V zero-error signal from the error amplifier.



Derivative action

Derivative action is achieved by placing network C6, R19 across the input resistor R18. When the temperature is changing the derivative capacitor C6 presents a low impedance which shunts R18 and increases the amplifier gain. With rapid input changes the capacitor C6 presents a short circuit and the amplifier gain is increased from $\frac{R20}{R18}$ to approximately $\frac{R20}{R19}$, assuming R19 has a much lower resistance than R18. The amplifier gain increases as the rate of change of temperature increases and the corresponding rapid change of output power acts in a direction which will reduce the rate of change of temperature. When the temperature is steady the derivative action dies away as C6 recharges through R18, R19. During warm-up when the temperature is a long way below set-point, T5 collector limits at 0V and causes C6 to charge by 4 volts. When the temperature reaches a point 40% of span below set point T5 collector starts to move negatively and the change is transmitted immediately to the three term amplifier by the charge on C6, giving normal derivative action 40% of span below set-point, provided the proportional band is set to maximum, and reducing the output power in proportion to the rate of rise of temperature. Derivative action will start to take effect 8% of span below set-point if the proportional band is set to minimum. Capacitor C8 also charges whilst T5 collector limits at 0V and is equivalent to moving the proportional band upscale. Discharge of the derivative capacitor C6, as the temperature rises, allows partial discharge of the integral capacitor C8, moving the proportional band downwards from its upscale position. This effect, combined with the derivative action, minimises temperature overshoot. The relative values of C6 and C8 are chosen to minimise overshoot without increasing warm-up time.



Desaturation network

Operation of normal derivative action outside the proportional band, as described above, is dependent on virtual-earth (-4V) conditions being maintained at the input to the three-term amplifier, since a saturated amplifier would be unable to act on the signal transmitted by C6. Transistors T6, T7 and associated components maintain a virtual-earth at the three-term amplifier input by switching additional feedback if the amplifier approaches saturation. The base of T7 is held at -9V. If T11 collector falls to -10V transistor T7 conducts and reduces the amplifier input by producing a voltage across R17. The base of T6 is held at -2V by potential divider R15, R16. If T11 collector rises to -1V transistor T6 conducts and reduces the amplifier input by producing a voltage across R17. Diodes D2 and D3 protect transistors T6 and T7 respectively from reverse voltage.

Power Supply

A reference voltage of -8.2V is provided across Z1 by the current through the mother-board resistor R11. Potential divider R33, R34 across Z1 provides a reference voltage of -3.3V at T13 base. Transistor T13 acts as an emitter-follower and provides a stabilised -4V supply at the emitter. The values of R33, R34 are chosen such that the negative temperature coefficient of T13 base-emitter junction compensates for the positive temperature coefficient of Z1, providing a temperature compensated -4V supply for the set point calibration board. Mains voltage compensation has to be provided for the stabilised -4V set-point supply, since a fall in mains voltage reduces the current through mother-board resistor R11 and causes a slight fall in the reference voltage across Z1. Compensation is achieved by resistor R31 on the amplifier board and resistor R9 on the mother-board. A fall in mains voltage produces a fall in current through R9. This reduces the voltage drop across R31 which compensates for the slight regulation of the -4V supply. Resistor R10 on the amplifier board provides similar mains voltage compensation for the error amplifier.

Time Constants

With proportional-only action the gain of the three term amplifier is equal to the ratio $\frac{R20}{R18}$ and this gain determines the bandwidth range of the controller. The standard 2% to 10% bandwidth is obtained with a three term amplifier gain of 5. Alternative 1% to 5% or 5% to 25% bandwidth ranges are obtained with gains of 10 or 2 respectively. With proportional plus derivative action the derivative time constant is equal to R18.C6 seconds, where R18 is in Megohms and C6 is in microfarads. With proportional plus integral action the integral time constant is equal to R20.C8 seconds. With three term, proportional plus derivative plus integral, action the amplifier gain and time constants alter slightly and are calculated as follows.

Integral time constant = T1 + T2 where T1 = R18.C6 T2 = R20.C8

$$\text{Derivative time constant} = \frac{T1.T2}{T1+T2}$$

$$\text{Amplifier gain} = \frac{R20}{R18} + \frac{C6}{C8}$$

The standard values T1 and T2 are 70 seconds and 330 seconds respectively, giving derivative and integral time constants of 60 seconds and 400 seconds respectively. The capacitors C6 and C8 are usually of equal value in order to provide an adequate amount of overshoot suppression, the amount of suppression increasing as the value of C6 is increased. The following tables show resistor and capacitor values required for various values of T1 and T2 with different proportional bandwidths.

PROPORTIONAL BAND 1% to 5% R18 = 15MΩ R20 = 150MΩ			
T1 DERIVATIVE	C6	T2 INTEGRAL	C8
3 SECS	.22	33 SECS	.22
7 SECS	.47	70 SECS	.47
15 SECS	1.0	150 SECS	1.0
33 SECS	2.2	330 SECS	2.2
50 SECS	3.3	500 SECS	3.3
70 SECS	4.7	700 SECS	4.7
100 SECS	6.8	1000 SECS	6.8

PROPORTIONAL BAND 2% to 10% R18 = 33MΩ R20 = 150MΩ			
T1 DERIVATIVE	C6	T2 INTEGRAL	C8
7 SECS	.22	33 SECS	.22
16 SECS	.47	70 SECS	.47
33 SECS	1.0	150 SECS	1.0
70 SECS	2.2	330 SECS	2.2
110 SECS	3.3	500 SECS	3.3
160 SECS	4.7	700 SECS	4.7
220 SECS	6.8	1000 SECS	6.8

PROPORTIONAL BAND 5% to 25% R18 = 75MΩ R20 = 150MΩ			
T1 DERIVATIVE	C6	T2 INTEGRAL	C8
16 SECS	.22	33 SECS	.22
35 SECS	.47	70 SECS	.47
75 SECS	1.0	150 SECS	1.0
160 SECS	2.2	330 SECS	2.2
250 SECS	3.3	500 SECS	3.3
350 SECS	4.7	700 SECS	4.7
500 SECS	6.8	1000 SECS	6.8

All capacitor values in ∕uF

System Stability

The standard 2% to 10% proportional bandwidth and the standard derivative and integral time constants of 60 seconds and 400 seconds respectively have been selected to give stable control over a very wide range of industrial applications. Should the control loop become unstable, resulting in a cyclic oscillation of the temperature, first increase the proportional bandwidth to maximum. If the oscillation continues after a period of several time constants, convert the controller to proportional action by opening link d1 - d2 and making link I1 - I2. The temperature will control downscale due to the absence of integral action. If the oscillation persists with the proportional band set to maximum, this indicates that the system gain is too high. An excessive heater rating or an oversized valve are typical causes of such instability. The proportional bandwidth of the controller can be increased if it is not possible to alter the external control parameters. When stable control is achieved, slowly narrow the proportional band until the system again becomes unstable, making one adjustment every 15 minutes. Note the period of oscillation, one undershoot plus one overshoot, and select a value of C8 which gives a T2 value approximately equal to the period of oscillation. Fit a derivative capacitor C6 of equal value and increase the proportional bandwidth by approximately 50%. Stable control should now be achieved. Equal capacitor values are chosen for C6 and C8 in order to give an adequate amount of overshoot suppression, the amount of suppression increasing as the value of C6 is increased. The controller must be converted to proportional action before the system oscillation period is measured, otherwise an incorrect result will be obtained. If the integral time constant is made too short the system will continue to oscillate. If the integral time constant is made too long the control will be stable but the system settling time will be increased.

Amplifier Adjustment and Checking

The following adjustment and checking procedure enables the main amplifier board to be fully checked as an individual board rather than as an integrated part of the complete controller. The amplifier board must be inserted in the mother board to pick up the power supplies but the other boards can be included or omitted as desired.

1. Insert the main amplifier board into the mother board and connect the mains supply. With a d.c. voltmeter connected to the OV terminal, check the -4V, -9V and -24V supplies and check the -8V reference at terminal X. A failure in the -9V or -24V supplies could be due to a fault on the mother board. Check the -4V supply between the -4V and 'stabilised OV' terminals.

2. Open link d1 - d2 located at the upper left corner of the board to remove derivative action. Make link I1 - I2 to remove integral action.

3. Link the junction of R19, R21 to the -4V supply to give a -4V input to the three term amplifier. Check that the auto-manual switch, if fitted, is set to 'auto' and that the power control P4 is set fully clockwise.

4. Place the d.c. voltmeter between the 'control signal' and OV terminals. Turn P3 anticlockwise and check that the control signal swings to approximately -9V. Turn P4 slowly anticlockwise and check that the control signal falls smoothly to -4V. Reset P4 to its fully clockwise position and check that the control signal rises smoothly to approximately -9V. Turn P3 clockwise and check that the control signal swings to approximately -1V. If an output board is inserted in the mother board this signal may limit at -3.5V due to inclusion of a clamping diode on the output board. Reconnect the voltmeter between the 'control signal' and -4V terminals and slowly adjust P3 to give a null on the voltmeter or to the point where the control signal just swings through the null point.

5. Remove the link from the junction of R19, R21. Link both inputs A and B to the -4V supply. Set the bandwidth potentiometer P1 fully clockwise.

6. Monitor the error amplifier output by connecting the voltmeter between the feedback and OV terminals. Turn P2 anticlockwise and check that the voltmeter reads approximately OV. Check that the temperature indicator is downscale (under temperature). Turn P1 anticlockwise and check that the voltmeter reading increases smoothly to approximately -3V, then reset P1 fully clockwise. Turn P2 clockwise and check that the amplifier output swings to approximately -9V and that the temperature indicator swings upscale.

7. Connect the voltmeter between the 'control signal' and OV terminals and check that the control signal swings from approximately -1V to approximately -9V as P2 is turned anticlockwise. This check confirms that the error amplifier signal is reaching the three term amplifier.

8. Connect the voltmeter between the feedback and -4V terminals and slowly adjust P2 to give a null on the voltmeter or to the point where the feedback signal just swings through the null point.

9. Disconnect the voltmeter. Remove the links from inputs A and B. Remove link I1 - I2 and remake link d1 - d2.

Incorrect adjustment of the potentiometers P2 and P3 results in a control offset when integral action is present. If the amplifier board is faulty the following voltage table can be used to locate the fault.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to OV using a 10V d.c. voltmeter having a resistance of 20KΩ/volt. The following test conditions must be satisfied. Remove link d1 - d2 and make link I1 - I2. Switch the auto-manual switch to the 'auto' position, if fitted. Set P4 fully clockwise. Remove the calibration board and arrange to link either input A or input B to -4V. . Remove the output board.

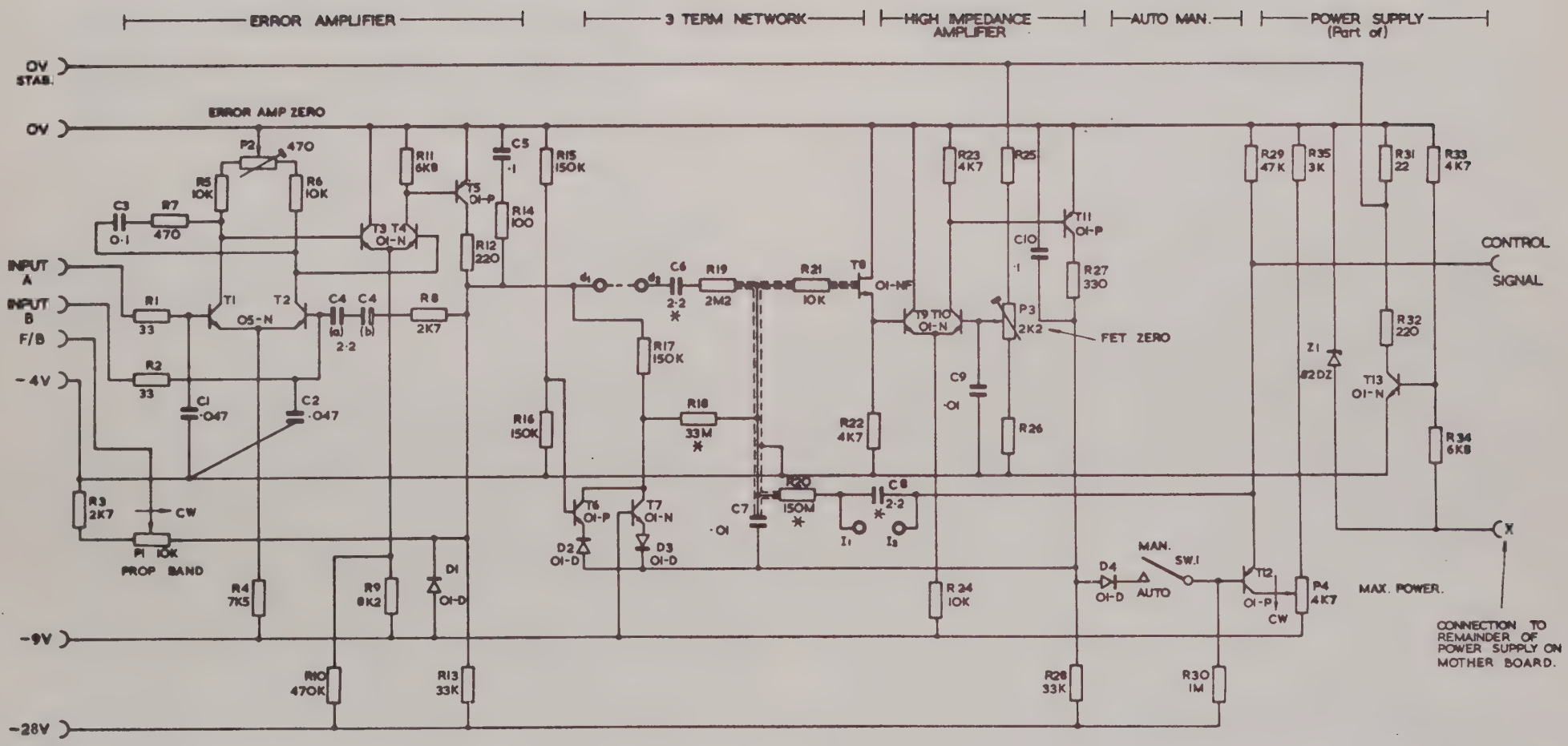
Observe test conditions given above.

	TEST CONDITION	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
EMITTER	INPUT A= -4V	-4.5	-4.5	-.8	-.8	0	-1.5	-9.3	-2.8	-3.3	-3.3	0	-8.7	-4
	INPUT B= -4V	-4.5	-4.5	-.6	-.6	0	-1.5	-.7	-2.8	-3.3	-3.3	0	-1	-4
BASE	INPUT A= -4V	-4	-4	-4.5	0	-.7	-1.5	-8.7	*	-2.8	-2.8	-.6	*	-3.3
	INPUT B= -4V	-4	-4	0	-4.5	0	-1.5	-8.7	*	-2.8	-2.8	-.6	*	-3.3
COLLECTOR	INPUT A= -4V	-4.5	0	0	-.7	0	-3	-3	0	0	-.6	-9.6	-8.7	-1
	INPUT B= -4V	0	-4.5	0	0	-9.3	-4.5	-4.5	0	0	-.6	-.6	-8.7	-1.2

All measurements in volts

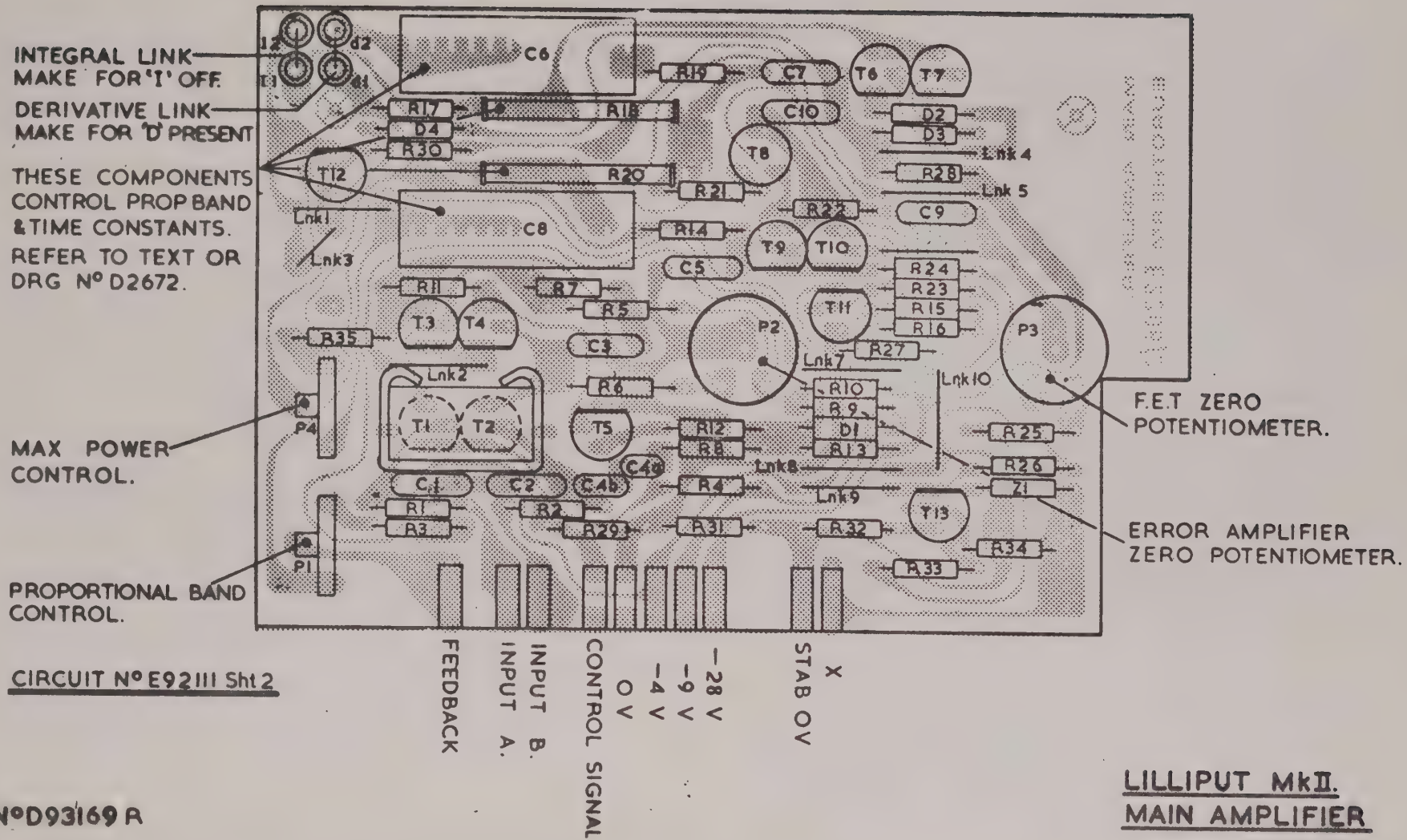
* Cannot be measured due to high circuit impedance.

Drg N° E9211 Sht 2. R



COMPONENTS MARKED THUS * VARY WITH MODE OF OPERATION.
REFER TO WRITE UP FOR DETAILS.
R25 & R26 ARE DEPENDENT UPON F.E.T. SEE DR'G N° C 4367
LAYOUT N° D9 3169

LILLIPUT Mk II.
MAIN AMPLIFIER.



CIRCUIT Nº E92111 Sht 2

Drg Nº D93169 A

LILLIPUT MkII.
MAIN AMPLIFIER

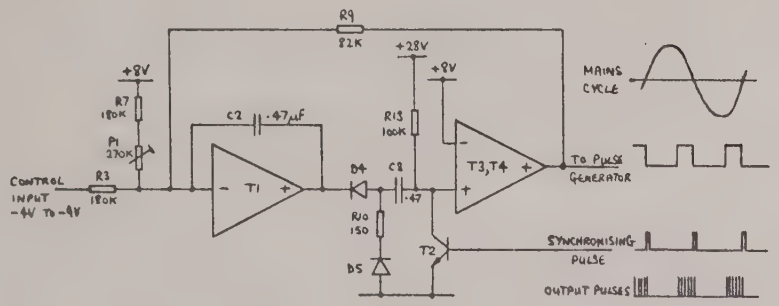
PHASE ANGLE PULSE OUTPUT BOARD

Function

The phase angle pulse output board converts a 0 to 5V d.c. input signal into trigger pulses suitable for driving thyristors in the phase angle mode.

Circuit Description

The input control signal operates between the levels -4V and -9V, corresponding respectively to minimum and maximum output power. The output pulses are generated during each half cycle of the mains supply, the phase or conduction angle advancing as the input power demand is increased. Power feedback provides compensation for mains voltage variations and provision is made for limiting the load current.



Transistor T2 is switched on for a short period at each zero voltage crossover point in the mains cycle, discharging C3 via T2, D5, R10. When T2 switches off both plates of C3 move positively, due to the presence of R13, until D4 becomes forward biased and one plate of C3 is clamped to the output potential of amplifier T1. In this condition D5 is reverse biased and the other plate of C3 ramps positively as C3 charges via R13. When C3 charges to +8.5V the comparator amplifier T3, T4 switches on the blocking oscillator T5, TX1 to provide thyristor trigger pulses at the output windings. The output of amplifier T3, T4 also provides feedback to the input of amplifier T1 via R9 whenever the oscillator is switched on. The output pulses cease when C3 is discharged at the end of each half cycle due to conduction of T2 and a further cycle commences. The time interval between the beginning of each half cycle and the commencement of output pulses is dependent on the potential at the output of amplifier T1. When the output at T1 collector is 0V, capacitor C13 cannot charge sufficiently during the 10mSec half-cycle to reach +8.5V and switch on the oscillator. When the output at T1 collector is +8.5Vthe output pulses commence as soon as T2 becomes non-conducting at the beginning of the half cycle.

With a control input of -4V the bias potentiometer P1 is adjusted so that the positive bias current through P1, R7 just exceeds the negative control current in R3, thereby holding T1 collector potential at 0V for inputs between 0V and -4V. With an input control signal between -4V and -9V the overall negative input current to T1 base causes T1 collector potential to ramp positively as the input current charges C2. As T1 collector potential rises positively the conduction angle of the thyristors and the feedback via R9 increase simultaneously. The conduction angle increases until the feedback current via R9 balances the input current through R3. Since the time constant of the integrator is long compared with the mains half cycle the signal at T1 collector achieves a steady value appropriate to the conduction angle. At maximum conduction angle the feedback current through R9 is just sufficient to balance a control input of -9V and the conduction angle is therefore proportional to the input signal over the input range -4V to -9V.

Capacitor C8 provides a +28V smoothed supply from the unsmoothed +24V board supply. Zener diode Z1 provides a stabilised +8V supply for the current limit, bias and comparator circuits. The input virtual earth at T1 base is held at approximately +.6V by T1 base-emitter junction. The potential divider R2, R1 provides a +.6V reference for the current limit input so that a current limit input voltage of only 100mV is sufficient to turn off the output pulses, even with maximum control input. Network R5, R6, C1, D1, D2 is a quench circuit which rapidly retards the conduction angle to zero in the event of an interruption of the mains supply, ensuring that conduction advances steadily from zero on reconnection of the supply and thereby avoiding undesirable current surges, particularly with transformer loads. Diode D1 is normally forward biased by the current through D1, causing D2 to remain reverse biased and establishing a small charge on C1 which prevents D2 from conducting momentarily each half cycle as the fall-wave rectified unsmoothed -24V supply falls to zero. If the mains supply is interrupted the -24V supply ceases immediately but the +28V supply remains due to the charge on C8. Diode D2 conducts and rapidly discharges C2, retarding the conduction angle to zero. Diode D3 limits the positive excursion at T1 collector under maximum power demand conditions to +8.5V, thereby allowing the quench circuit to be fully effective for all conduction angles.

Network D6, R11, R12 provides synchronising pulses to make T2 conduct for a short period at each crossover point in the mains cycle, the base of T2 becoming positive as the -24V unsmoothed supply falls to zero. Diode D6 limits the reverse emitter-base voltage applied to T2. The base of T4 is held at +8V by Z1 so that T4 conducts and turns on the pulse generator when the ramp on C3 reaches +8.5V. Diode D7 prevents reverse emitter-base conduction of T4 when T2 conducts.

Power Feedback

Due to the square law relationship between voltage and power a 10% rise in mains voltage will cause a 20% rise in load power unless the conduction angle of the thyristors reduces to compensate for the change. A 10% rise in mains voltage produces a 10% rise in the +28V supply across C8, causing the current in R14 to increase. The corresponding increase in T4 collector current causes an increase in the feedback voltage applied to R9 when output pulses are present, causing the conduction angle to reduce until the average feedback voltage reduces to its previous level and thereby compensating for the rise in mains voltage.

Pulse Generator

The blocking oscillator formed by T5, TX1 and associated components provides thyristor trigger pulses at the output windings whenever T4 conducts. The pulses have an amplitude of 10 volts, a duration of 12 uSec and a repetition rate of four pulses per millisecond. When T4 conducts transistor T5 is biased into conduction by the base current through R22, R17, T5 and the primary of TX1. The voltage appearing across the primary winding of TX1 reflects an additional bias voltage across C7, R18 in such direction that the conduction of T5 is increased. The regenerative action of C7, R18 causes the conduction of T5 to increase to saturation, applying 28V across the primary of the transformer and producing a bias voltage of 6 volts and an output of 10 volts as defined by the turns ratio of the transformer. Capacitor C7 charges via T5 base and R18 after approximately 12 uSec and T5 then begins to switch off. The voltage across the transformer primary starts to reduce and the regenerative action of the bias winding causes T5 to switch off rapidly due to the charge on C7. When conduction in T5 ceases the inductance of the transformer causes the primary voltage to reverse. Diode D9 and resistor R19 provide a path for the inductive current to protect T5 from excessive voltage and prevent a subsequent large negative pulse at the output. Capacitor C7 discharges via R18, R17, R22 until T5 is again biased into conduction after approximately 250 uSec, generating a further 12 uSec pulse at the output. The action continues until T4 switches off at the end of the half cycle and the oscillator is biased off by the -.6V signal produced at D8 cathode by R15. Capacitor C4 provides some smoothing of the feedback via R9 and C5 prevents spurious triggering of the oscillator due to noise.

Checking

1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -24V, -28V and +28V supplies with a d.c. voltmeter. Failure of any of the power supplies could be due to a mother board fault.

2. Connect a 10V d.c. voltmeter between the control input and 0V terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.

3. Set the input control signal to -4V and monitor one output winding with an oscilloscope. Turn P1 anticlockwise until pulses appear at the output. Check that the amplitude of pulses is approximately 10 volts and that the polarity is as indicated. If this output is correct check the second output winding. Turn P1 clockwise until the pulses just cease with a control input of -4V applied. Check that the number of output pulses increases gradually as the input control signal is increased towards -9V. Check that output pulses occur over approximately 90% of each half cycle with a control input of -9V.

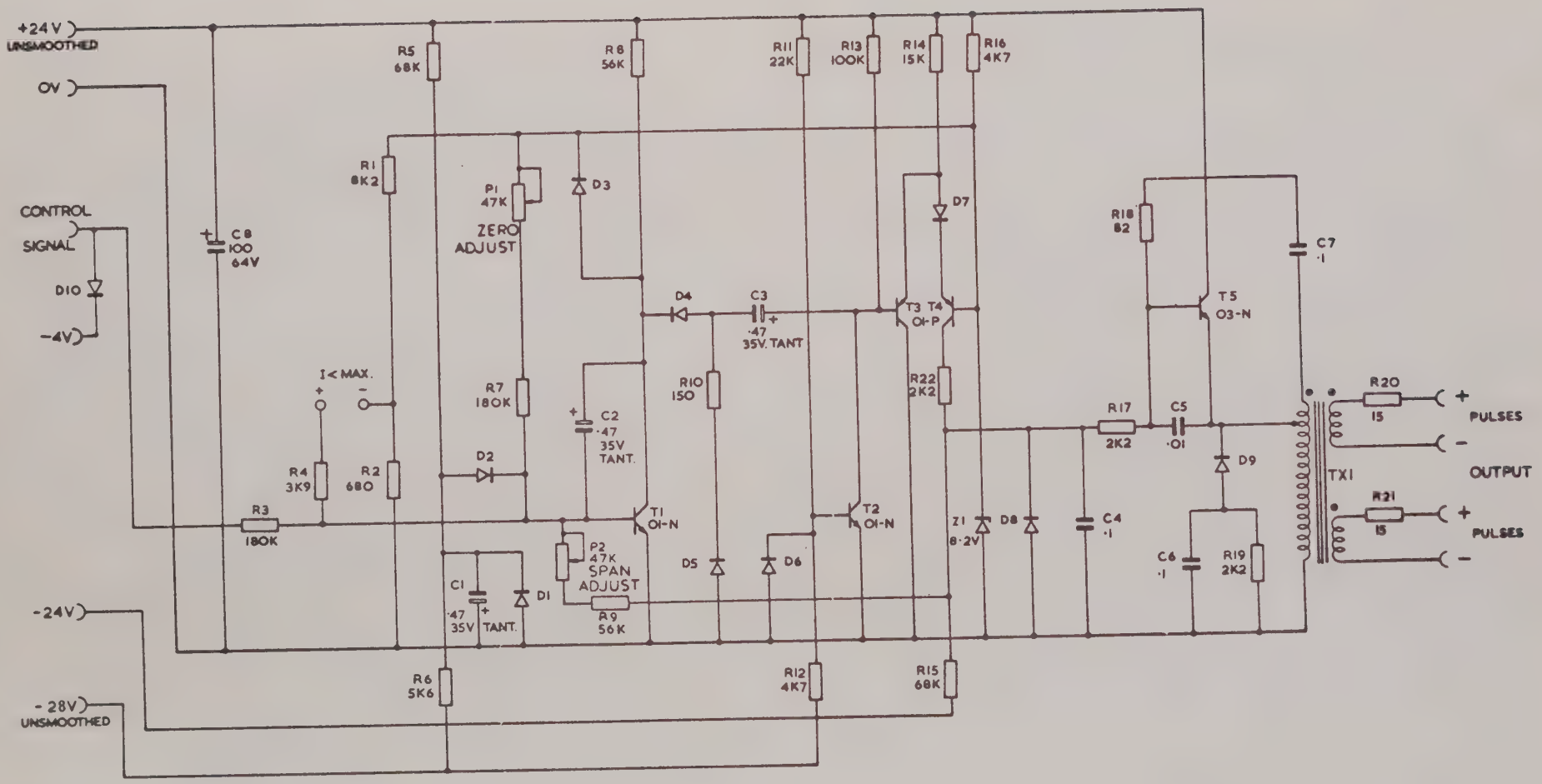
4. If the board does not function correctly first check the +8V supply across Z1 and then connect the d.c. voltmeter between 0V and T1 collector. The collector potential should increase from between 0V and +2V with a -4V control input to +8V with a -9V control input. If this is correct, connect the oscilloscope between 0V and the base of T2. A positive pulse of amplitude 1.5V and duration 1 mSec should occur once every 10 mSec if the mains supply is 50 c/s. If this is correct, connect the oscilloscope between 0V and the collector of T2. The waveform should be a positive ramp which returns to 0V at every crossover point in the mains cycle (every 10 mSec for a 50 c/s supply). The d.c. level at which the ramp commences should increase as the input control signal is increased from -4V to -9V. If this is correct, connect the oscilloscope between 0V and the collector of T4. The waveform should be a square wave of amplitude 5 volts, the positive period increasing from zero to approximately 90% as the input control signal is increased from -4V to -9V. Some 3 volts of high frequency oscillation will be superimposed on the positive part of the waveform due to the action of the blocking oscillator. If the waveform at T4 collector is normal and the pulse output is not, check operation of T5 and the output blocking oscillator. The d.c. voltage table will assist in locating faults, particularly if an oscilloscope is not available.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

	CONTROL INPUT	T1	T2	T3	T4	T5
EMITTER	-4V	0V	0V	+8V*	+5.5V*	0V
	-9V	0V	0V	+8V	+7.5V	0V
BASE	-4V	+.6V	-.5V	+5V*	+8V	-.5V
	-9V	+.6V	-.5V	+10V*	+8V	-.7V
COLLECTOR	-4V	+2V*	+5V*	0V	-.5V*	+30V
	-9V	+8V*	+10V*	0V	+4V	+30V

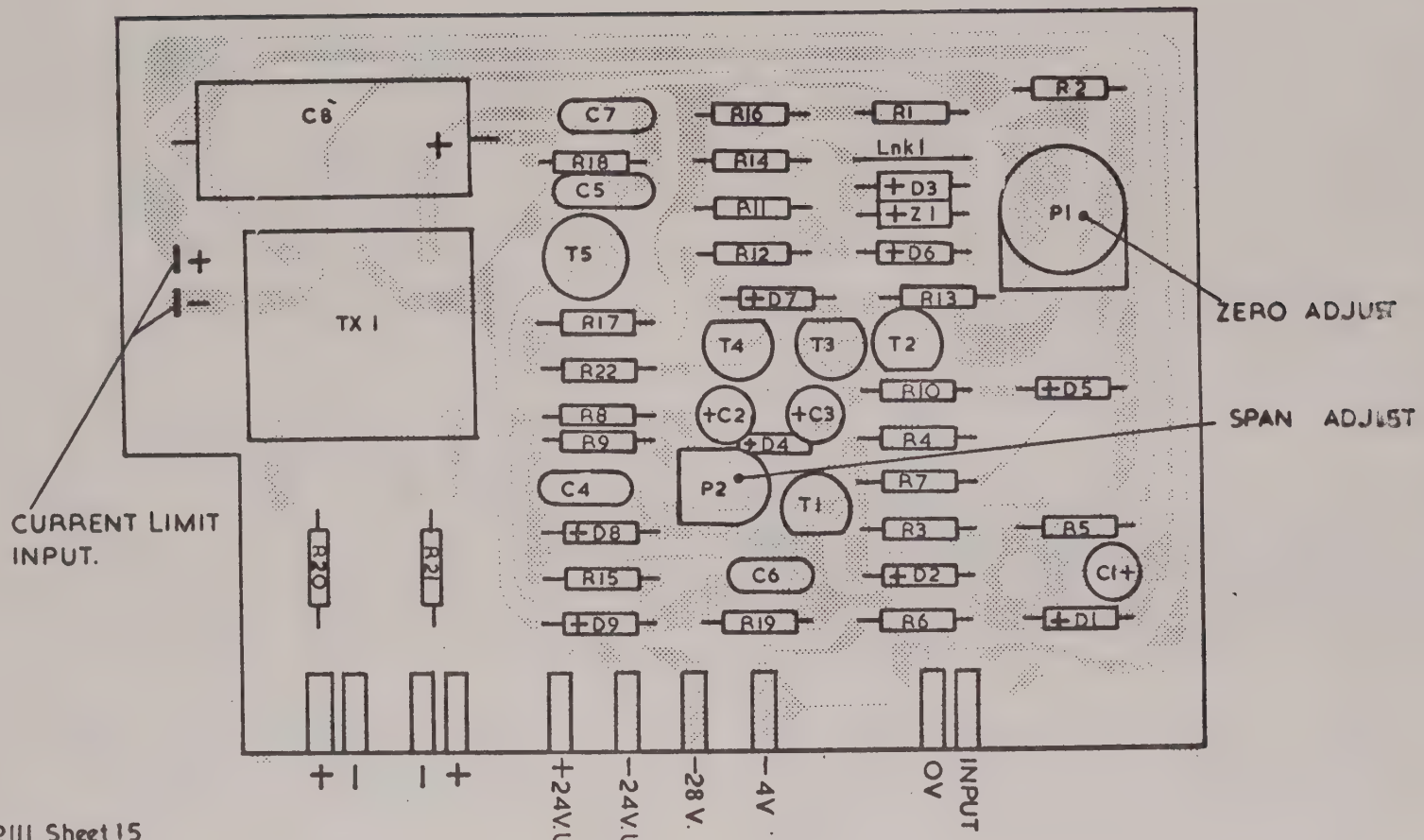
* These voltages are dependent on setting of P1
All voltages measured with reference to 0V using a d.c. voltmeter having a resistance of 20KΩ/volt



LAYOUT Nº D93253

LILLIPUT MkII.
PHASE ANGLE OUTPUT

Drg Nº E92111 Sht 15



CIRCUIT Nº E92111 Sheet 15

Drg Nº D93253

LILLIPUT MkII

PHASE ANGLE OUTPUT

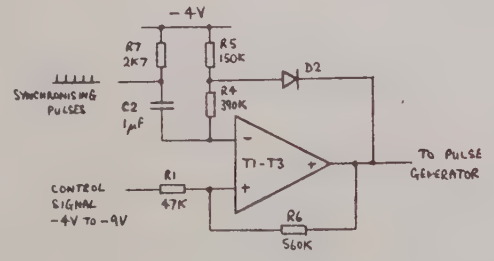
FAST CYCLE PULSE OUTPUT BOARD

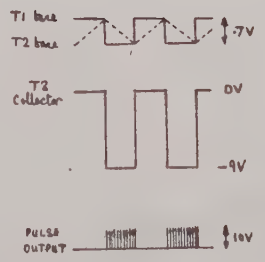
Function

The fast cycle pulse output board converts a 0 to 5V d.c. input signal into trigger pulses suitable for driving thyristors.

Circuit Description

The input control signal operates between the levels -4V and -9V, corresponding respectively to minimum and maximum output power. The output pulses are generated on a time proportioning basis with an ON + OFF period of approximately 120 + 120 mSec at half power. The commencement of trigger pulses is synchronised to the zero voltage crossover point of the mains cycle to minimise interference. Power feedback is employed so that the load power remains constant if the mains voltage varies.





Transistors T1 to T3 and associated components form a high-gain d.c. amplifier with overall positive gain from T1 base to T3 collector and positive feedback via R6. With an input control signal of -7V to R1, transistors T1 and T3 switch off and the collector of T3 falls to a potential of approximately -9V as defined by resistors R9, R10. Positive feedback via R6 causes the potential at T1 base to fall to -7.2V. Diode D2 conducts, causing capacitor C2 to charge negatively towards -9V (T3 collector potential) via R4. When C2 has charged to -7.2V, transistors T1 and T3 conduct and T3 collector potential rises to 0V. Positive feedback via R6 causes T1 base potential to rise to -6.5V, ensuring that T1 and T3 remain hard on. Diode D2 is reverse biased and C2 commences to discharge towards -4V via R4, R5, R7. Capacitor C2 discharges to -6.5V after approximately 120mSec, at which point transistors T1 and T3 switch off. The positive feedback via R6 causes T1 base potential to fall again to -7.2V and capacitor C2 charges negatively from -6.5V towards -9V (T3 collector potential) via R4, D2. Capacitor C2 charges to -7.2V after approximately 120 mSec, at which point T1 and T3 conduct and the cycle is repeated. With an input control signal of -7V capacitor C2 thus charges and discharges continually between the levels -6.5V and -7.2V, producing a square wave of period approximately 120 + 120 mSec and magnitude approximately 9 volts at T3 collector. The output oscillator switches ON whenever T3 collector is negative, producing trigger pulses at the output windings of the transformer.

The ON - OFF switching differential of .7V at T1 base remains approximately constant as the input control signal varies, but the switching level follows the control signal. As the input control signal becomes more negative the average level of charge on C2 becomes more negative, causing the charging current via D2 to decrease and the discharge current to increase. This gives an increasing output ON time and a decreasing output OFF time until the output oscillator stays permanently ON when the control signal becomes more negative than T3 collector potential (approximately -9V). As the input control signal becomes less negative the output ON time decreases and the OFF time increases until the output oscillator stays permanently OFF with an input control signal of less than -4V.

Synchronisation

The commencement of the ON period of the output pulses is synchronised to the zero voltage crossover point of the mains cycle by components R7, R8, D1, D3. The negative full-wave-rectified unsmoothed waveform at D3 cathode produces a positive pulse of approximately .2V magnitude across R7 at each crossover point in the mains cycle due to conduction of D1 when the waveform falls to zero. This positive pulse is transmitted to T2 base via C2 and this synchronises the commencement of output pulses to the crossover point in the mains cycle. The controller and load supplies must be from the same phase of the mains supply for the synchronisation to be effective.

Power Feedback

Due to the square law relationship between voltage and power, a 10% rise in mains voltage will produce a 20% rise in load power unless the output ON time reduces to compensate for the change. A 10% rise in mains voltage causes a 10% rise in the smooth, but unstabilised, -28V supply. This produces a 10% change in T3 collector voltage from -9V to -9.9V during the period when the output oscillator is ON. The increased charging current through R4, D2 reduces the output ON time by approximately 20% and this compensates for the change in supply voltage.

Pulse Generator

The blocking oscillator formed by T4, TX1 and associated components provides thyristor trigger pulses at the output windings whenever T3 collector potential falls to -9V. The pulses have an amplitude of 10 volts, a duration of 12μSec and a repetition rate of four pulses per millisecond. When T3 collector falls to -9V transistor T4 is biased into conduction by the base current through D4, R11, R12. The voltage appearing across the primary winding of TX1 reflects an additional bias voltage across C6, R13 in such direction that the conduction of T4 is increased. The regenerative action of C6, R13 causes the conduction of T4 to increase to saturation, applying 28V across the primary of the transformer and producing a bias voltage of 6 volts and an output of 10 volts as defined by the turns ratio of the transformer. Capacitor C6 charges via T4 base and R13 after approximately 12μSec and T4 then begins to switch off. The voltage across the transformer primary starts to reduce and the regenerative action of the bias winding causes T4 to switch off rapidly due to the charge on C6. When conduction in T4 ceases the inductance of the transformer causes the primary voltage to reverse. Diode D5 and resistor R14 provide a path for the inductive current to protect T4 from excessive voltage and prevent a subsequent large negative pulse at the output. Capacitor C6 discharges via R11, R12, R13 until T4 is again biased into conduction after approximately 250μSec, generating a further 12μSec pulse at the output. The

action continues until T3 collector potential rises to 0V. Capacitor C3 prevents the pulses from reaching T3 collector and C4 prevents spurious triggering of the oscillator due to noise.

Checking

1) With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V, -24V and -28V supplies with a d.c. voltmeter. Failure of any of the supplies could be due to a mother board or amplifier board fault.

2) Connect a 10V d.c. voltmeter between the control input and 0V terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.

3) Set the input control signal to -6.5V and monitor one output winding with an oscilloscope. Bursts of pulses, of magnitude 10 volts and polarity as shown, should be present at the output. The ON + OFF period should be approximately 100 + 100 mSec. If this output is correct check the second output winding. Check that the ON time decreases as the control input is reduced to -4V. Check that the ON time increases as the control input is increased to -9V.

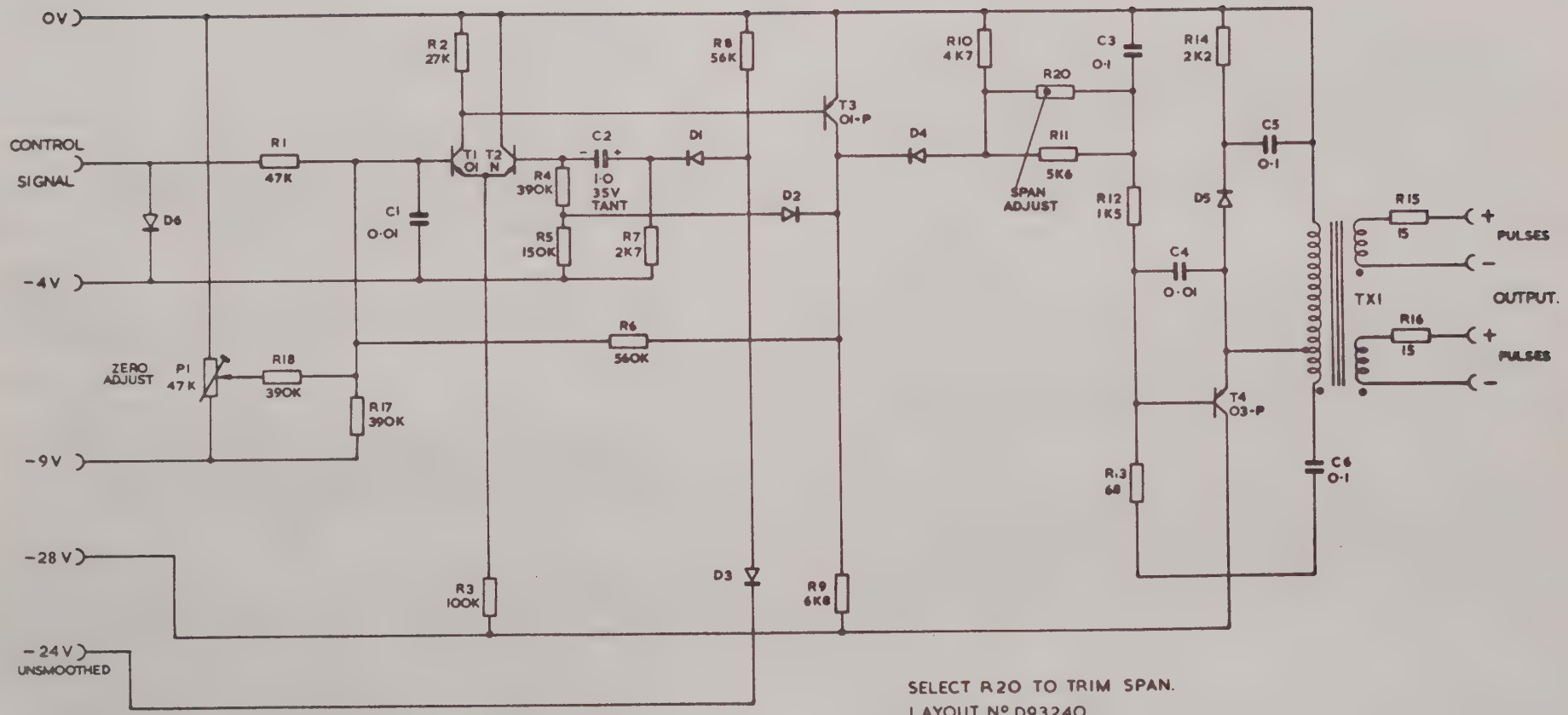
4) If no pulses are present at the output, set the control input to -6.5V and monitor the signal at T3 collector with the oscilloscope. This should be a square wave of period approximately 100 + 100 mSec switching between 0V and -9V. If this square wave is present check operation of T4 and the output blocking oscillator. If the square wave is not present at T3 collector check operation of T1, T2, T3. The d.c. voltage table will assist in locating the fault.

D.C. Voltage Table

Typical d.c. voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

	CONTROL INPUT	T1	T2	T3	T4
EMITTER	-4V	-4.5V	-4.5V	0V	0V
	-9V	-9V	-9V	0V	0V
BASE	-4V	-4V*	-4V*	-.7V	0V
	-9V	-9V*	-9V*	0V	+.5V
COLLECTOR	-4V	-.7V	0V	0V	-28V
	-9V	0V	0V	-9V	-28V

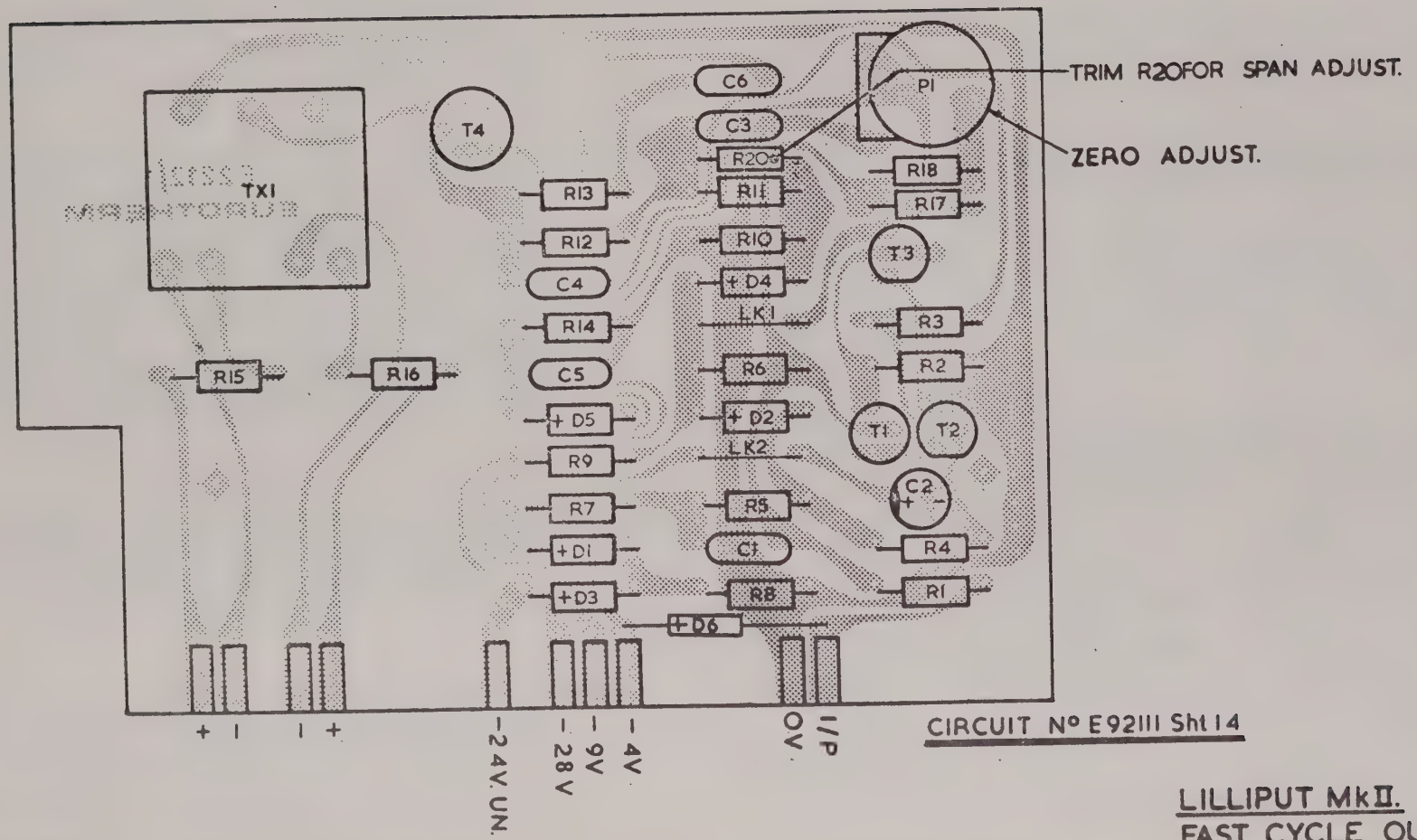
* Must be measured with an oscilloscope or an electronic voltmeter due to high circuit resistance.
All other measurements may be taken with a d.c. voltmeter having a resistance of 20Kn/volt.
All voltages measured with reference to 0V.



SELECT R20 TO TRIM SPAN.
LAYOUT Nº D93240

LILLIPUT MkII.
FAST CYCLE OUTPUT.

Drg NºE92111 Sht14 R



Drg Nº D93240R

LILLIPUT MkII.
FAST CYCLE OUTPUT.

ISOLATED 5 VOLT OUTPUT BOARD

Function

The 5 volt output board converts a 0 to 5 volt d.c. input into an electrically isolated 0 to 5 volt d.c. output with a current rating of .25mA.

Circuit Description

The input control signal operates between the levels -4V and -9V. The board is able to operate in two modes, normal or inverted, by changing links on the printed circuit board. In the normal mode, intended for heating applications, a control input of -4V corresponds to zero output and a control input of -9V corresponds to 5 volts output. In the inverted mode, intended for cooling applications where the output board is used in the parent controller, a control input of -4V corresponds to 4.5 volts output and a control input of -8.5V corresponds to zero output. The output is proportional to the input over the working range.

The oscillator consisting of T3, TX1 and associated components derives its supply from the emitter followers T1, T2. The oscillator supply thus appears across the smoothing capacitor C2 and the peak value of the oscillation is only slightly less than the voltage across C2 (the peak to peak voltage is twice this value). The secondary winding has a few more turns than the primary winding so that the secondary peak voltage is equal to the voltage across C2. The peak-rectifying and smoothing network D1, C5 thus produces a d.c. voltage at the output which is .5V less than the d.c. voltage across C2, the difference being due to the turnover voltage of D1. Transistor T3 is biased into conduction by the current through R8, the base drive being proportional to the oscillator supply voltage across C2. Positive feedback to T3 base via C4, R9 and the bias winding of TX1 causes the circuit to oscillate. The frequency of oscillation is fixed at approximately 30Kc/s by the parallel tuned circuit consisting of C3 and the primary inductance of TX1. The oscillation is sinusoidal. Resistor R10 provides base drive to T3 when the voltage across C2 is small, ensuring that oscillation commences at very low applied voltages. Resistor R7 limits T3 peak collector current.

Normal Mode

The emitter potential of T2 is fixed at approximately -4V by the potential divider R3, R4. The emitter potential of T1 follows the input control signal and varies between -4.5V and -9.5V as the input signal is varied between -4V and -9V. The oscillator supply across C2 thus varies between .5 volt and 5.5 volts as the input signal is varied between -4V and -9V. Since the primary and secondary voltages are equal and the volt drop across D1 is .5 volt, the d.c. output signal varies from zero to 5 volts as the input signal is varied from -4V to -9V.

Inverted Mode

The emitter potential of T1 is fixed at -9.5V by its base connection to the -9V supply. The emitter potential of T2 follows the input control signal and varies between -4.5V and -9.5V as the input signal is varied between -4V and -9V. The oscillator supply across C2 thus varies between 5 volts and zero as the input signal is varied between -4V and -9V. Since the primary and secondary voltages are equal and the volt drop across D1 is .5 volt, the d.c. output signal varies from 4.5 volts to zero as the input signal is varied from -4V to -8.5V.

Checking

1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V and -28V supplies. Failure of a power supply could be due to a fault on the mother board or the amplifier board.

2. Connect a 10V d.c. voltmeter between the control input and 0V terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board. Place a 22KΩ resistor across the output.

3. If the board is connected in the normal mode set the control input to -9V and check that a 5 volt output, of the correct polarity, is obtained at the output. Gradually reduce the input control signal to -4V and check that the output reduces proportionally to within .3 volt of zero output. If the output does not reduce sufficiently shunt R3 with an appropriate resistor in the space provided on the printed circuit board.

4. If the board is connected in the inverted mode set the control input to -4V and check that a 4.5 volt output, of the correct polarity, is obtained at the output. Gradually increase in the input control signal to -8.5V and check that the output reduces proportionally to zero.

5. If no output is obtained, first check C5, D1 and the continuity of the output winding. Check that the voltage across C2 varies between approximately zero and 5 volt as the input signal is varied and then check the oscillator. If the output is not controllable, first check that a variable voltage is obtained across C2 as the input signal is varied. The d.c. voltage table will assist in locating the fault. Note that due to the low value of R7 a fault on T3 may affect the previous stages.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

NORMAL MODE

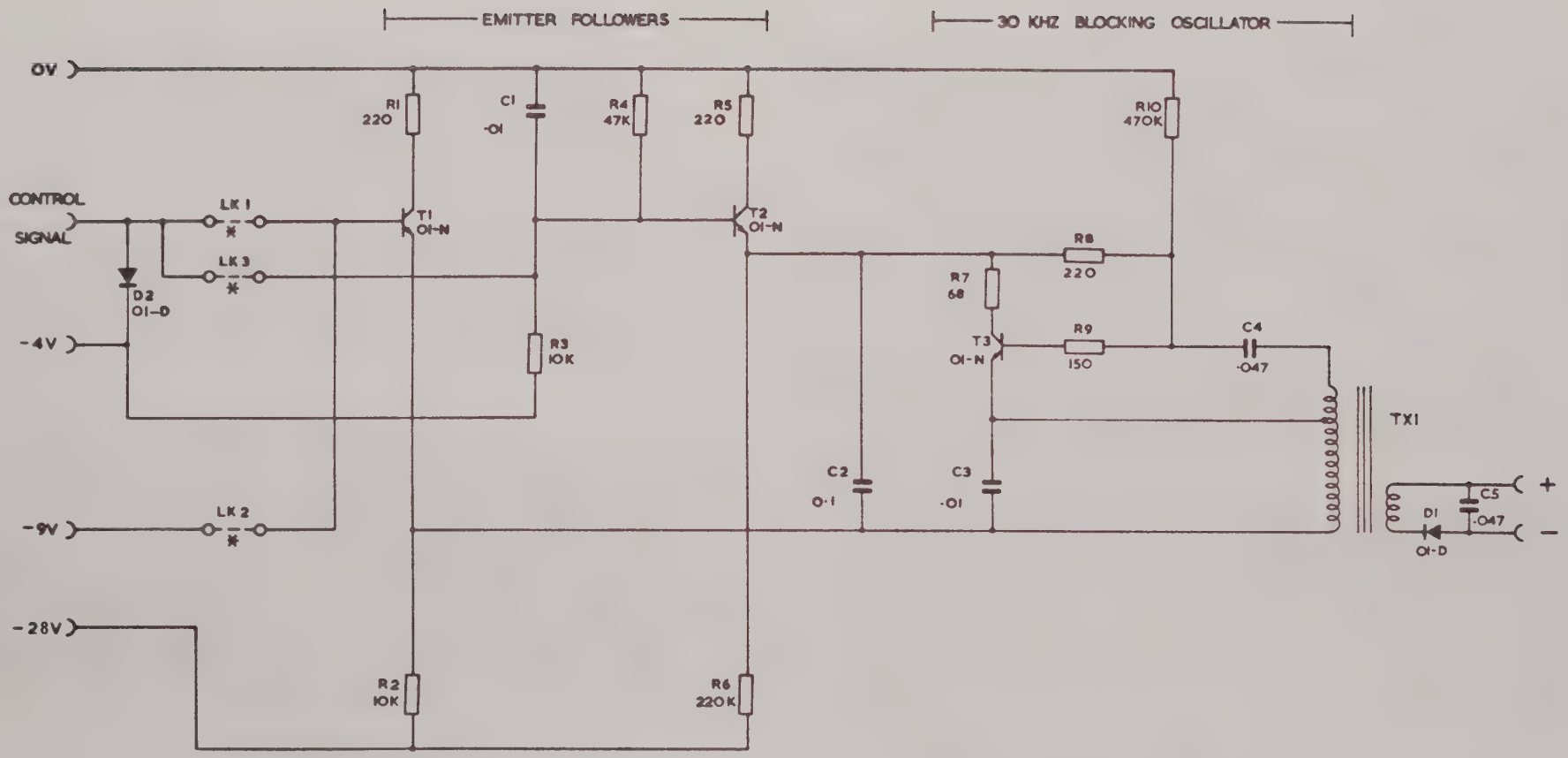
	CONTROL INPUT	T1	T2	T3
EMITTER	-4V	-4.5V	-3.8V	-4.5V
	-9V	-9.5V	-3.8V	-9.5V
BASE	-4V	-4V	-3V	-4V*
	-9V	-9V	-3V	-9V*
COLLECTOR	-4V	-.5V	0V	-3.8V
	-9V	-.4V	0V	-3.8V

INVERTED MODE

	CONTROL INPUT	T1	T2	T3
EMITTER	-4V	-9.5V	-4.5V	-9.5V
	-9V	-9.5V	-9.5V	-9.5V
BASE	-4V	-9V	-4V	-9V*
	-9V	-9V	-9V	-9V*
COLLECTOR	-4V	-.4V	0V	-4.5V
	-9V	-.3V	0V	-9.5V

All voltages measured with reference to 0V with a 10V d.c. voltmeter having a resistance of 20KΩ/volt.

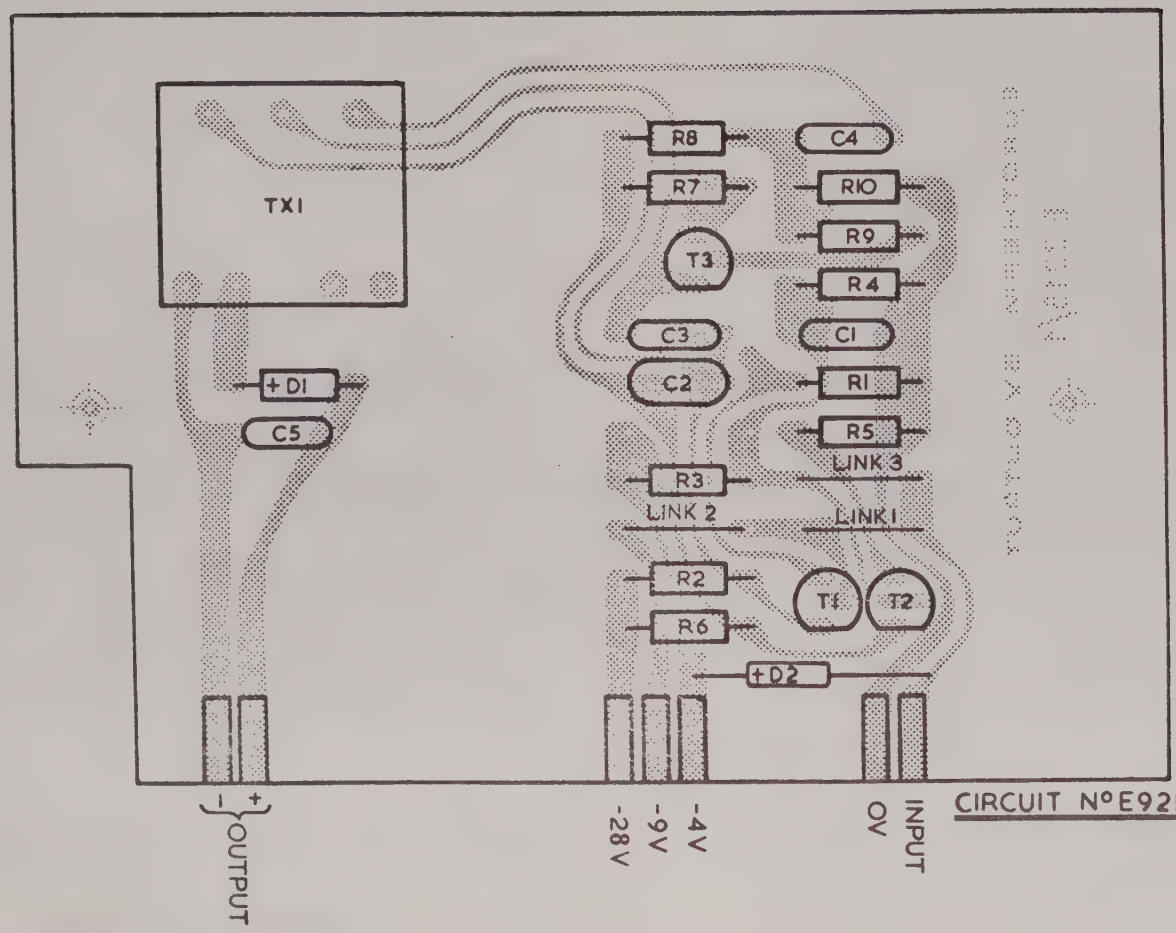
* Voltmeter current at this point may cause the oscillation to cease.



LINKS MARKED * VARY WITH MODE OF OPERATION.
REFER TO WRITE UP FOR DETAILS.
LAYOUT Nº D93255

LILLIPUT Mk II.
ISOLATED 5V OUTPUT.

DRG Nº E92m Sht 16 R



1. FOR NORMAL HEAT OPERATION LK1 IS MADE & LKS 2 & 3 OMITTED.
2. FOR INVERTED OUTPUT (COOL) LINK 1 OMITTED. LINK 2 MADE. LINK 3 MADE.

CIRCUIT Nº E92111 Sht 16

LILLIPUT Mk II
ISOLATED 5V OUTPUT.

Drg Nº D93255 R

ISOLATED MILLIAMP OUTPUT BOARD

Function

The isolated milliamp output board converts a 0 to 5 volt d.c. input into an electrically isolated 0 to 10 mA (20V) current output or a 0 to 20mA (12V) current output or a 0 to 5V (10mA) voltage output.

Circuit Description

The input control signal operates between the levels -4V and -9V. For normal operation links 12 and 13 are made and inputs of -4V and -9V correspond respectively to minimum and maximum output. By making links 11 and 14 instead of links 12 and 13 an inverted operating mode is achieved where inputs of 14V and 19V correspond respectively to maximum and minimum output. Output of 0 to 5V, 0 to 10mA or 0 to 20mA in either mode are achieved by suitable selection of R31, R34, R35, LK1, LK2, LK3, LK4 as indicated on the circuit diagram. Outputs of 1 to 5V, 2 to 10mA or 4 to 20mA are achieved by suitable selection of R3, R4, R5 as indicated on the circuit diagram.

The input control signal is fed via emitter-followers T1 and T2 onto the control oscillator consisting of T3, TX1 and associated components. The control oscillator produces an isolated d.c. voltage across C4 which is proportional to the input control signal. In the normal mode a -4V control input corresponds to minimum voltage across C4 (zero or 1 volt depending on output range) and an input voltage of -9V corresponds to 5 volts across C4. The buffer amplifier T8 to T10 and associated components converts the 0 to 5 volt (or 1 to 5 volt) signal across C4 into a 0 to 10mA (or 2 to 10mA) current signal with an output voltage capability of 20 volts. Current outputs of 0 to 20mA or 4 to 20mA with an output voltage capability in excess of 12 volts can also be provided by suitable component selection. Alternatively the 0 to 5 volt (or 1 to 5 volt) signal across C4, which has a current capability of only .25mA, can be converted to a 0 to 5 volt (or 1 to 5 volt) signal with an output current capability of 10mA. To give complete output isolation an isolated 28 volt buffer supply is provided via a d.c. to d.c. converter consisting of transistors T4 to T7, transformer TX2, diodes D4 to D7 and associated components.

The control oscillator T3, TX1, detailed operation of which is described later, produces an output d.c. voltage across C4 which is .5 volt less than the input d.c. voltage across C1 due to the turnover voltage of diode D2. Diode D1 is included in the emitter circuit of T1 to balance out the effect of D2 and make the output voltage across C4 equal to the potential difference between the bases of T1 and T2. The buffer, consisting of T8, T9, T10 and associated components, is a sign-reversing feedback amplifier with overall gain from input (junction C4, R26) to output (junction R31, R35) defined by $-\frac{R31}{R26}$. When R26 and R31 have equal values of 47KΩ a -5 volt signal across C4 produces a + 5 volt signal across R35 and the 5 volt output signal is taken from across R35 by making links 2 and 4. When a current output is required R31 is reduced to 15Ω to give 1.5 volts across R35 with 5 volts across C4. The value of R35 is chosen to produce the desired output current (150Ω for 10mA or 75Ω for 20mA) and the output current is taken from the collector circuit by making links 1 and 3. Network C9, R24, D8 provides smoothing of the isolated 28V buffer supply without direct capacitive loading of the converter, since direct capacitive loading could cause the converter action to cease. Resistor R24 provides a suitable charging impedance for C9 and diode D8 provides a low impedance discharge path to maintain the buffer supply whilst the converter switches at the end of each half cycle. Resistor R27 provides h.f. interference rejection. Components C10, C11, R30 provide h.f. feedback stabilisation for amplifier T1, T2. Resistors R32, R33 are h.f. stoppers and resistor R34 provides output short circuit protection when the output is 0 to 5 volts. Diode D9 protects T10 from excessive forward voltage when the current output is used to drive an inductive load.

Control Oscillator

The control oscillator consisting of T3, TX1 and associated components is biased into conduction by current through R11, giving base drive to T3 which is proportional to the oscillator supply voltage across C1. Positive feedback to T3 base via C3, R12 and the bias winding of TX1 causes the circuit to oscillate sinusoidally at a frequency of 30kc/s defined by the parallel tuned circuit consisting of C2 and the primary inductance of TX1. Resistor R13 provides base drive to T3 when the voltage across C1 is small, ensuring that oscillation commences at very low applied voltages. Resistor R10 limits T3 peak collector current. The peak value of oscillation on the primary of TX1 is only slightly less than the oscillator supply voltage across C1 (the peak to peak voltage is twice this value). The secondary winding has a few more turns than the primary winding so that the secondary peak voltage is equal to the voltage across C1. The peak-rectifying and smoothing network D2, C4 thus gives an isolated d.c. control voltage which is .5 volt less than the d.c. voltage across C1 due to the turnover voltage of D2.

Supply Converter

The self-oscillating d.c. to d.c. converter consisting of transistors T4 to T7, transformer TX2 and associated components provides a 4Kc/s square wave of peak to peak amplitude 28 volts across the primary of TX2. A square wave of peak to peak amplitude 70 volts is reflected in the secondary winding of TX2, providing an isolated d.c. supply of approximately 32 volts via diodes D4 to D7. At maximum loading of 20mA the isolated supply voltage falls to approximately 24 volts due to regulation of the -28V instrument supply and regulation of the converter. The converter consists essentially of transistors T4 and T7, transformer TX2 and capacitors C7 and C8. One side of TX2 primary is held at -14V by voltage sharing capacitors C7, C8 and the other side of TX2 primary is switched alternately between 0V and -28V due to alternate conduction of T4 and T7. Voltage sharing capacitors are used to ensure that no d.c. component is present in the primary current of TX2. When T4 conducts, positive feedback to T4 base via R17 and the primary bias winding ensures that T4 remains hard 'on' and T7 remains 'off'. When T7 conducts, positive feedback to T7 base via C5, R20 ensures that T7 remains hard 'on' and T4 remains 'off'. In the absence of T5, T6 the 'on' time of transistors T4 and T7 would be determined by the saturation time of the transformer core. Transistors T5, T6 are included to drive the converter at a higher frequency than would result from saturation commutation, thereby avoiding excessive peak currents in transistors T4 and T7 at the end of each half cycle. The frequency of oscillation is fixed at 4Kc/s by capacitor C6 in association with resistors R15, R16, R18. The action is as follows. When T4 conducts the common emitters of T4, T7 rise to 0V and the bias winding gives a +3.5V supply at junction R17, C5. Transistor T4 is thus held hard 'on' by base current through R17 and transistor T7 is held 'off'. Junction C6, R18 rises initially to +7.5V due to the 4 volt charge acquired on C6 during the previous half cycle, thus holding transistor T5 'off'. Capacitor C6 recharges via R15, R18 until junction C6, R18 falls to a potential of -.5V, at which point T5 begins to conduct and the drive to T4 base is removed. When

conduction in T4 ceases, the primary voltage of TX2 reverses and positive feedback to T7 base via the bias winding and C5, R20 ensures that T7 is driven hard 'on', thus applying -28V to the primary winding of TX2. Junction C6, R18 falls initially to -35.5V and T7 remains 'on' until C6 recharges to -27.5V via R16, R18, at which point conduction of T6 removes the base drive to T7 and the cycle repeats continually. Unity mark to space ratio is achieved by providing equal charge and discharge paths for C6 via R15, R18 and R16, R18. Unity mark to space ratio in conjunction with the decoupling action of C7, C8 ensures positive and negative half cycles of equal magnitude and duration. Components C5, R19, R23 are included to ensure satisfactory self-starting of the converter by biasing T4 into conduction when the supply voltage is connected. Diode D3 prevents charging of C5 due to rectification at T7 base and thereby ensures that full drive is applied to T7 via R20 during the negative half cycle. Resistors R21 and R22 are h.f. stoppers which also provide a degree of current-limit protection for T4 and T7 during start-up. Resistor R14 prevents converter current from circulating through the instrument power supplies, the primary current for TX2 being drawn from C7 when T4 conducts and from C8 when T7 conducts. For all normal uses the two secondary windings of TX2 are connected in series by making links 5 and 8. This gives an isolated d.c. supply voltage of approximately 24 volts at maximum loading of 20mA. By making links 6 and 8 instead of links 5 and 8 a 0 to 50mA (6V max.) current output can be provided.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are given in the table for operation in the normal mode with a 0 to 10mA output. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

NORMAL MODE WITH 0 to 10mA OUTPUT

	CONTROL INPUT	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
EMITTER	-4V	-4.6V	-4.8V	- 5.3V	-14 V	-14.5V	-14 V	-14 V	+ .6V	0 V	0 V
	-9V	-9.3V	-4.8V	-10 V	-13.5V	-13.5V	-13.5V	-13.5V	+ .6V	0 V	+1.5V
BASE	-4V	-4 V	-4 V	- 4.7V*	-14.5V	-14.5V	-14.5V	-14 V	0 V	+ .6V	0 V
	-9V	-8.5V	-4 V	- 9.7V*	-13.5V	-12.5V	-12.5V	-13.5V	0 V	+ .6V	+2.1V
COLLECTOR	-4V	- .3V	- .1V	- 5 V	- .1V	-14 V	-14 V	-28 V	0 V	0 V	+32 V
	-9V	- .2V	- .1V	- 5 V	- .3V	-13.5V	-13.5V	-27 V	0 V	+2.2V	+28 V

All voltages measured with a d.c. voltmeter having a resistance of 20KΩ/volt
All voltages measured with reference to 0V, except for T8, T9, T10 whose voltages are measured with reference to T8 collector. The output load was a short circuit.

* Voltmeter current at this point may cause the oscillation to cease.

Checking

1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V and -28V supplies. Failure of a power supply could be due to a fault on the mother board or the amplifier board.

2. Connect a 10V d.c. voltmeter between the control input and 0V terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.

3. Check the board as follows depending on the type of output

   0 to 10mA or 2 to 10mA output

   Place a 1.8KΩ resistor and a 10mA d.c. meter in series across the output terminals. If the board is connected in the normal mode check that the output increases gradually from 0 to 10mA (or from 2 to 10mA) as the control input is increased from -4V to -9V. If the board is connected in the inverted mode check that the output increases gradually from 0 to 10mA (or 2 to 10mA) as the control input is reduced from -9V to -4V.

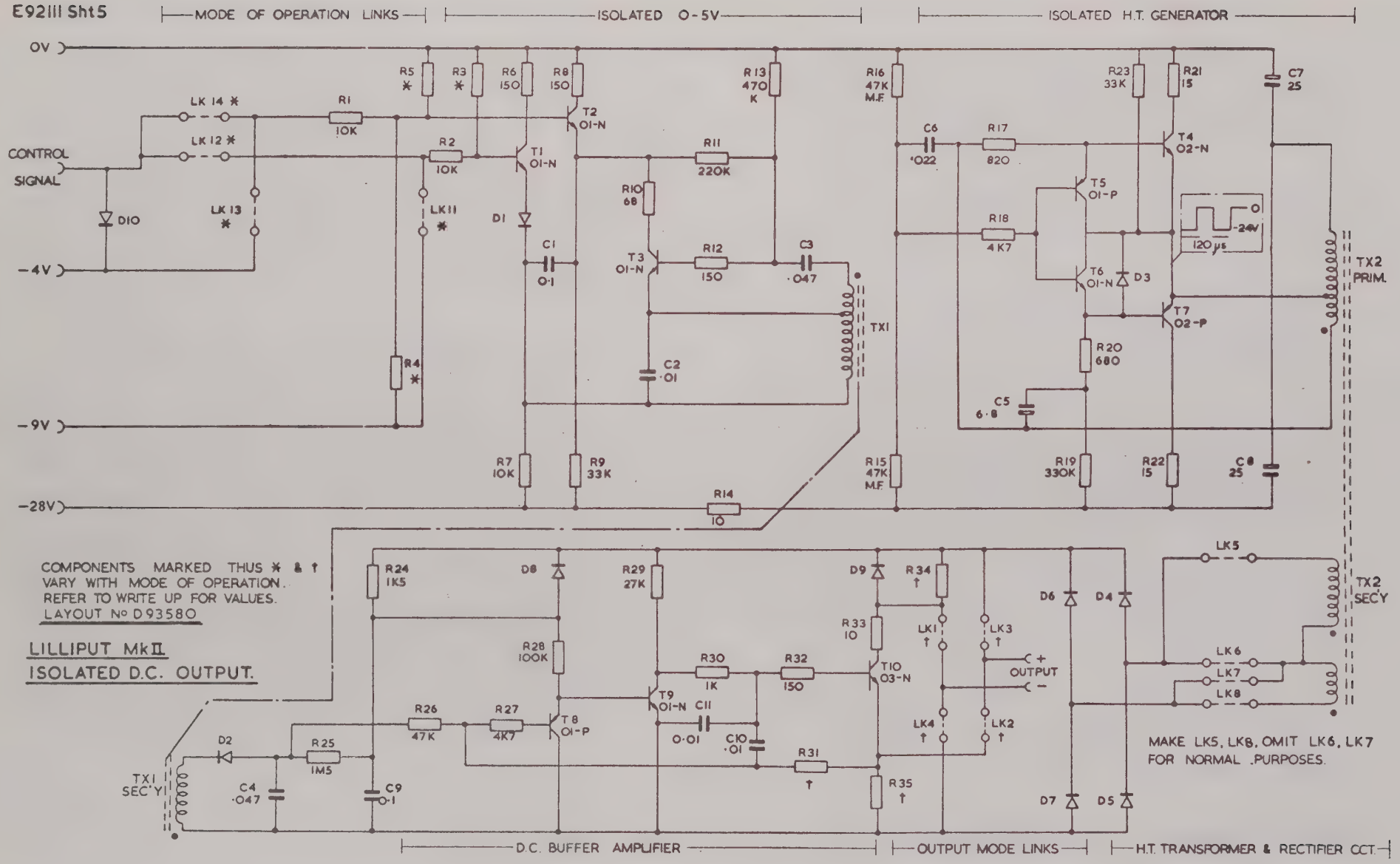
   0 to 20mA or 4 to 20mA output

   Place a 680Ω resistor and a 20mA d.c. meter in series across the output terminals. If the board is connected in the normal mode check that the output increases gradually from 0 to 20mA (or from 4 to 20mA) as the control input is increased from -4V to -9V. If the board is connected in the inverted mode check that the output increases gradually from 0 to 20mA (or 4 to 20mA) as the control input is reduced from -9V to -4V.

   0 to 5 volt or 1 to 5 volt output

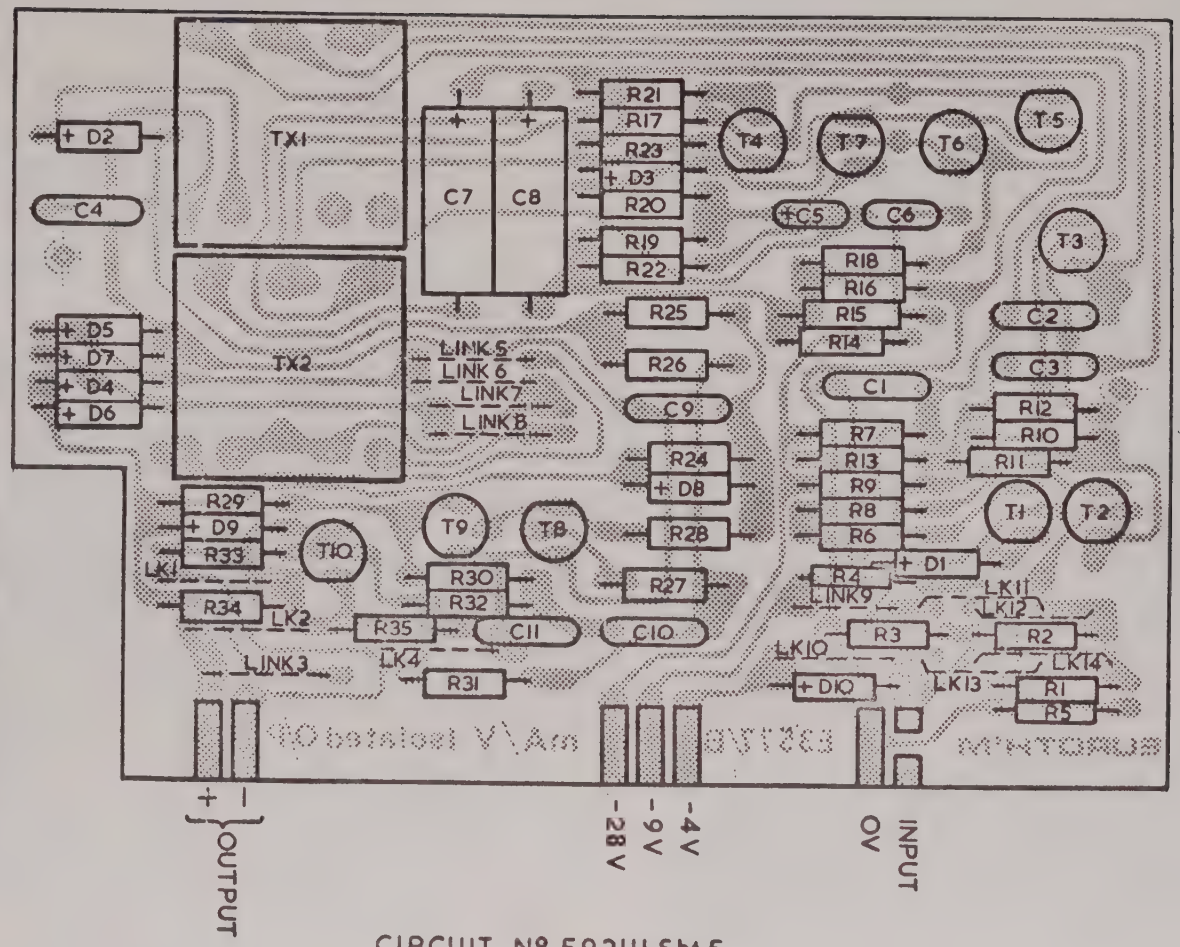
   Place a 470Ω resistor and a 10V d.c . voltmeter in parallel across the output terminals. If the board is connected in the normal mode check that the output increases gradually from 0 to 5 volt (or from 1 to 5 volts) as the control input is increased from -4V to -9V. If the board is connected in the inverted mode check that the output increases gradually from 0 to 5 volts (or 1 to 5 volts) as the control input is reduced from -9V to -4V.

4. If no output is obtained first check the isolated 28 volt buffer supply between D7 anode (-) and D6 cathode (+). This should be between 22 volts and 36 volts depending on the output load and mains voltage. If this supply is present next check that the voltage across C1 varies between approximately .5 volt and 5.5 volts as the input signal is varied between -4V and -9V. Check that the voltage at junction C4, R26 varies between zero and -5 volts, with reference to T8 collector, as the input signal is varied between -4V and -9V. If the board is connected for current output, check that the voltage at junction R31, R35 varies between zero and +1.5 volts, with reference to T8 collector, as the input signal is varied between -4V and -9V. If the board is connected for 5 volt output, check that the voltage at junction R31, R35 varies between zero and +5 volts, with reference to T8 collector, as the input signal is varied between -4V and -9V. The d.c. voltage table will assist in locating any fault.


E92111 Sht5
MODE OF OPERATION LINKS
ISOLATED 0-5V
ISOLATED H.T. GENERATOR
0V
-4V
-9V
-28V
CONTROL SIGNAL
LK 14 *
LK 12 *
LK 13 *
LK11 *
R1 10K
R2 10K
R3 *
R4 *
R5 *
R6 150
R7 10K
R8 150
R9 33K
R10 68
R11 220K
R12 150
R13 470 K
R14 10
R15 47K M.F.
R16 47K M.F.
R17 820
R18 4K7
R19 330K
R20 680
R21 15
R22 15
R23 33K
C1 0·1
C2 ·01
C3 ·047
C5 6·8
C6 ·022
C7 25
C8 25
D1
D3
D10
T1 01-N
T2 01-N
T3 01-N
T4 02-N
T5 01-P
T6 01-N
T7 02-P
TX1
TX2 PRIM.
0
-24V
120 µs
COMPONENTS MARKED THUS * & † VARY WITH MODE OF OPERATION. REFER TO WRITE UP FOR VALUES. LAYOUT No D93580
LILLIPUT MkII
ISOLATED D.C. OUTPUT.
R24 1K5
R25 1M5
R26 47K
R27 4K7
R28 100K
R29 27K
R30 1K
R31 †
R32 150
R33 10
R34 †
R35 †
C4 ·047
C9 ·1
C10 ·01
C11 0·01
D2
D4
D5
D6
D7
D8
D9
T8 01-P
T9 01-N
T10 03-N
TX1 SEC'Y
LK1 †
LK2 †
LK3 †
LK4 †
LK5
LK6
LK7
LK8
+ OUTPUT -
TX2 SEC'Y
MAKE LK5, LK8, OMIT LK6, LK7 FOR NORMAL PURPOSES.
D.C. BUFFER AMPLIFIER
OUTPUT MODE LINKS
H.T. TRANSFORMER & RECTIFIER CCT.

INPUT	Lnk11	Lnk12	Lnk13	Lnk14	R3	R4	R5
0-100%	—	✓	✓	—	—	120K	—
20-100%	—	✓	✓	—	39K	—	18K
100-0 %	✓	—	—	✓	220K	—	—
100-20%	✓	—	—	✓	68K	—	39K

OUTPUT	Lnk1	Lnk 2	Lnk 3	Lnk 4	R31	R34	R35
10mA. Max	✓	—	✓	—	15K	—	150
20mA "	✓	—	✓	—	15K	—	75
5 V "	—	✓	—	✓	56K	820	1K
10 V "	—	✓	—	✓	120K	560	22K



CIRCUIT Nº E92111 Sht 5.

Drg Nº D93580

LILLIPUT Mk II,
ISOLATED D.C.OUTPUT.

DUAL 5 VOLT OUTPUT BOARD

Function

The dual 5 volt output board converts a 0 to 6.5 volt d.c. input into two electrically isolated 0 to 5 volt d.c. outputs with a current rating of .25mA. The board has a special input-output characteristic intended for heat-cool applications.

The input control signal operates between the levels -2V and -8.5V. An input of -2V corresponds to maximum 5 volt cool output and zero heat output. An input of -8.5V corresponds to zero cool output and maximum 5 volt heat output. The input-output characteristic is such that the cooling output falls gradually to zero as the input signal becomes more negative and the heat output then increases gradually from zero. The changeover from cooling to heating can be made to occur anywhere within the input signal range -4V to -7V by adjusting the rear-access 'relative-bandwidth' control P1. The heat and cool outputs can be made to overlap by up to 5% at the changeover point by adjusting the rear access 'overlap' or 'crossover' control P4.

Relative bandwidth

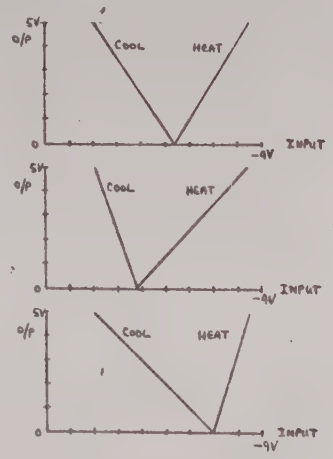
The setting of the proportional band potentiometer P1 on the main amplifier board defines the amplifier input change, expressed as a percentage of span, required to give an amplifier output change from -4V to -8.7V, these two levels corresponding to zero and maximum output respectively for the majority of output boards. Since the dual 5 volt board requires a control signal change from -2V to -8.5V to give an output change from maximum cooling to maximum heating, the total bandwidth between the maximum cooling and maximum heating points is 1.4Xp where Xp is the amplifier bandwidth setting.

For satisfactory heat-cool operation the heat channel gain, expressed in watts per degree change, should be matched to the cool channel gain. The relative bandwidth control enables the heat channel gain to be increased as the cool channel gain is decreased, and vice-versa. This enables the heat and cool channels to be matched provided the external parameters of the separate channels do not differ by a factor of more than 10:1.

With the relative bandwidth control P1 set midway the heat and cool channel bandwidths are equal at approximately .7Xp and crossover occurs at an input of approximately -5.5V.

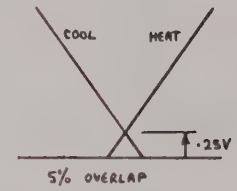
With the relative bandwidth control P1 set fully anticlockwise the heat channel bandwidth is approximately three times wider than the cool channel bandwidth and crossover occurs at an input of approximately -4V.

With the relative bandwidth control P1 set fully clockwise the cool channel bandwidth is approximately three times wider than the heat channel bandwidth and crossover occurs at an input of approximately -7V.

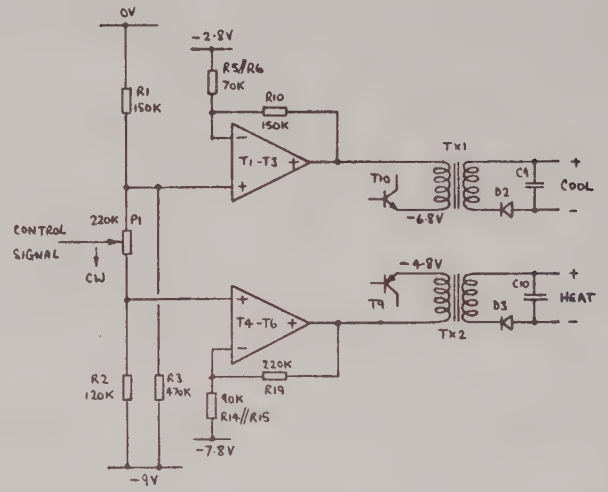


Overlap

Some overlap of the heat and cool channels is provided so that the effect of any external driver imperfection or channel gain mismatch can be minimised in the crossover region. With the overlap or crossover control P4 set fully anticlockwise there is no overlap and the heat output increases from zero as soon as the cool output falls to zero. With the overlap control set fully clockwise there is 5% of overlap of heat and cool channels, an output of .25 volt being present on both channels at the crossover point.



Circuit Description



The cool oscillator consisting of T7, TX1 and associated components derives its negative supply from emitter follower T10 and its positive supply from the cool amplifier consisting of T1 to T3 and associated components. The heat oscillator consisting of T8, TX2 and associated components derives its positive supply from emitter follower T9 and its negative supply from the heat amplifier consisting of T4 to T6 and associated components. The oscillators have equal primary and secondary turns and the output voltage is thus equal to the oscillator supply voltage minus the .5V diode drop. With zero overlap the emitter potentials of T10 and T9 are held respectively at -6.8V and -4.8V.

The cool amplifier has a positive gain of 3.2 from T1 base to T3 collector, as defined by the values of R5, R6, R10. A reference potential of -2.8V is provided at T2 base by potential divider R5, R6. A potential of -2.1V at T1 base corresponds to a cool amplifier output of -.6V, a cool oscillator supply of 6.2 volts and a cool output of 5.7 volts. With maximum output loading of .25mA

the cool output decreases to 5 volts due to regulation. A potential of -3.8V at T1 base corresponds to a cool amplifier output of -6.3V, a cool oscillator supply of .5 volt and a cool output of zero. With maximum load the cool output thus decreases from 5 volts to zero as the potential at T1 base falls from -2.1V to -3.8V.

The heat amplifier has a positive gain of 3.5 from T4 base to T6 collector, as defined by R14, R15, R19. A reference potential of -7.8V is provided at T5 base by potential divider R14, R15. A potential of -7V at T4 base corresponds to a heat amplifier output of -5.3V, a heat oscillator supply of .5 volt and a heat output of zero. A potential of -8.5V at T4 base corresponds to a heat amplifier output of -10.3V, a heat oscillator supply of 5.5 volts and a heat output of 5 volts. The heat output thus increases from zero to 5 volts as the potential of T4 base falls from -7V to -8.5V.

The input network consisting of P1, R1, R2, R3 holds the bases of T1 and T4 at -3.8V and -7V respectively in the absence of an input signal i.e. with the input open circuit. The heat and cool channels are therefore both biased to a point where they are just giving zero output. When a control signal is applied to the wiper of P1, a positive shift in the base potentials of T1 and T4 causes the cool output to increase and the heat output to remain at zero and a negative shift in the base potentials of T1 and T4 causes the heat output to increase and the cool output to remain at zero. The influence of the control signal on the bases of T1 and T4 is dependent on the setting of P1 due to the potential divider action of P1 with R1 and R2. The relative gains of the heat and cool channels are thus dependent on the setting of P1.

When the resistance of the overlap control P4 is set to maximum the emitter potential of T9 is shifted positively by .25 volt and the emitter potential of T10 is shifted negatively by .25 volt. With no input signal applied the output on both heat and cool channels is thus .25 volt, giving 5% overlap of heat and cool outputs.

The cool oscillator consisting of T7, TX1 and associated components is biased into conduction by current through R26, giving base drive to T7 which is proportional to the oscillator supply voltage across C3, provided the voltage across C3 is of the correct polarity. Positive feedback to T7 base via C7, R27 and the bias winding of TX1 causes the circuit to oscillate sinusoidally at a frequency of 30Kc/s defined by the parallel tuned circuit consisting of C5 and the primary inductance of TX1. Resistor R30 provides base drive to T7 when the voltage across C3 is small ensuring that oscillation commences at very low applied voltages. Resistor R24 limits T7 peak collector current. The peak value of oscillation on the primary of TX1 is only slightly less than the oscillator supply voltage across C3 (the peak to peak voltage is twice this value). The secondary winding has a few more turns than the primary winding so that the secondary peak voltage is equal to the voltage across C3. The peak-rectifying and smoothing network D2, C9 thus gives a d.c. cool output voltage which is .5 volt less than the d.c. voltage across C3 due to the turnover voltage of D2. The heat oscillator operates in a similar manner.

Adjustment

The adjustment potentiometers P2 and P3 are factory set and should not be disturbed unnecessarily. If adjustment is necessary the following procedure must be adopted.

1. Open circuit the control signal input by opening the link on the output board. Insert the output board into the mother board and ensure that the main amplifier board is also present.

2. Place a d.c. voltmeter across each of the 5 volt outputs and apply the normal load to each output. Set the 'crossover' or 'overlap' control P4 fully clockwise.

3. Connect the supply and adjust P2 until equal readings are obtained on both outputs. Adjust P3 until the sum of the output readings is equal to .5 volt. Re-adjust P2 and P3 until an output of .25 volt is obtained simultaneously on each channel.

4. Remake the control signal link and set P4 fully anticlockwise.

Checking

1. With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -9V and -28V supplies. Failure of a power supply could be due to a fault on the mother board or the amplifier board.

2. Connect a 10V d.c. voltmeter between the control input and 0V terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.

3. Place a 10V d.c. voltmeter across each of the 5 volt outputs and apply the normal load to each output. Set the 'relative bandwidth' control P1 to its mid position. Set the 'overlap' or 'crossover' control P4 fully anticlockwise.

4. With a control input of -9V the heat output should be approximately 5 volts. As the control input is reduced the heat output should reduce gradually to zero and the cool output should then increase gradually from zero to approximately 2 volts as the control input is reduced to -4V.

5. Set the control input to give approximately zero output on both channels. Check that there is no deadband between the heat and cool channels. Turn the 'overlap' control P4 fully clockwise and check that simultaneous readings of approximately .25 volt can be obtained on both channels. Reset P4 fully anticlockwise.

6. Turn the 'relative bandwidth' control P1 clockwise and check that the cool output increases smoothly to approximately 1.5 volts. Turn P1 anticlockwise and check that the heat output increases smoothly to approximately 1.5 volts. Reset P1 to its mid position.

7. Open circuit the controller input and check that the cool output increases to approximately 5 volts after a short delay.

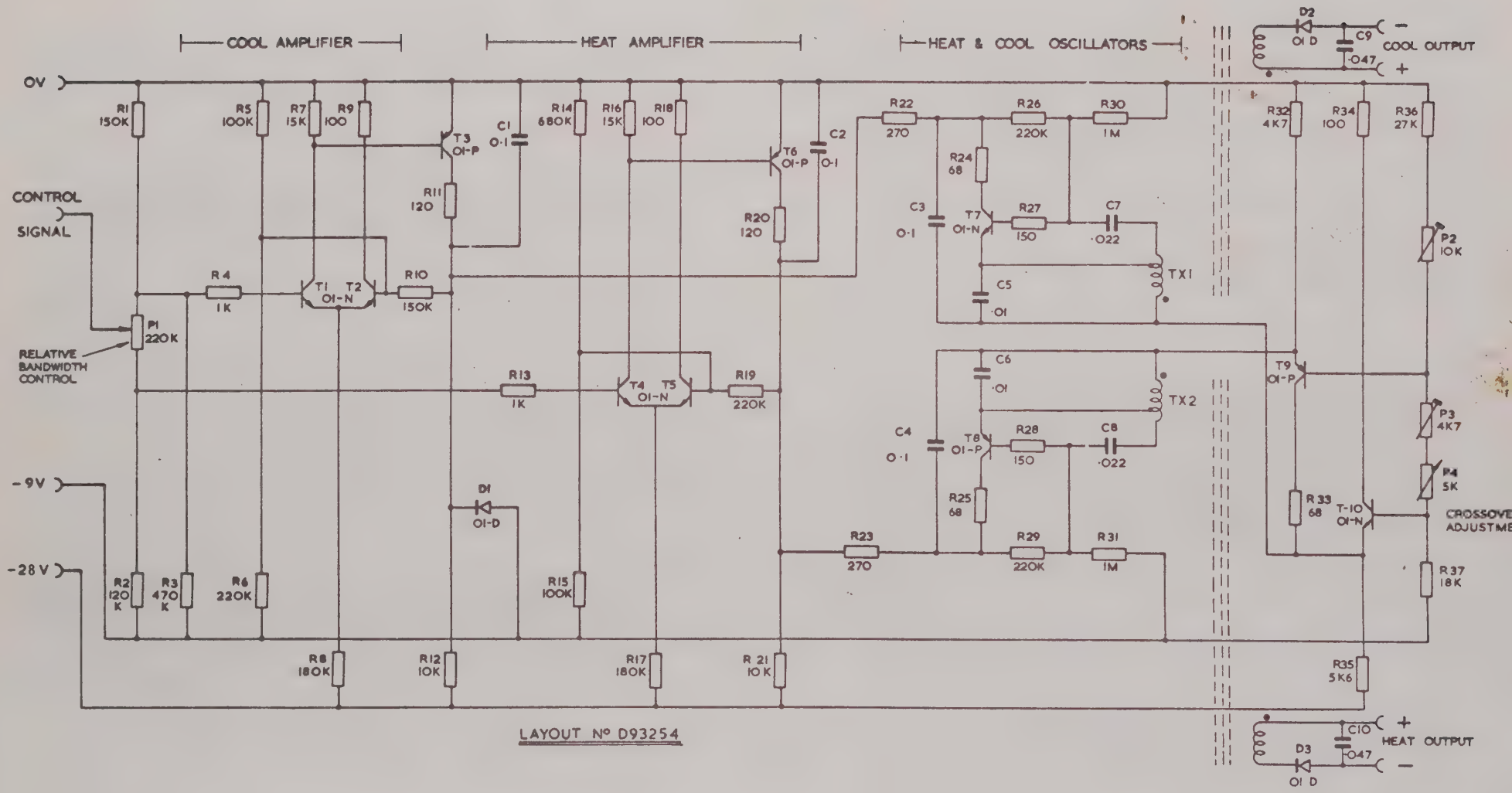
8. If no output is obtained from either channel, first check the continuity of the output winding then check the peak rectifying components D2, C9 or D3, C10 as appropriate. Check that the voltage across the appropriate oscillator smoothing capacitor C3 or C4 varies as the input signal is varied. Check that the oscillator is functioning normally. The d.c. voltage table will assist in locating any fault.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are given in the table. With the output board and the main amplifier board inserted in the mother board demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input. Set the 'relative bandwidth' control P1 to its mid position and the 'overlap' or 'crossover' control P4 fully anticlockwise.

	CONTROL INPUT	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
EMITTER	-4V	-3.6V	-3.6V	0 V	-6.8V	-6.8V	0 V	- 6.7V	- 4.8V	-4.8V	-6.7V
	-9V	-6 V	-6 V	0 V	-9.2V	-9.2V	0 V	- 6.7V	- 4.8V	-4.8V	-6.7V
BASE	-4V	-3 V*	-3 V*	- .6V	-6.2V*	-6.2V*	- .6V			-5.3V*	-6.1V*
	-9V	-5.4V*	-5.4V*	- .6V	-8.6V*	-8.6V*	- .6V			-5.3V*	-6.1V*
COLLECTOR	-4V	- .6V	0 V	- 3.8V	- .6V	0 V	- 2.9V	- 3.9V	- 2.9V	-6.7V	- .3V
	-9V	- .6V	0 V	-11 V	- .6V	0 V	-11 V	-11 V	-11 V	-6.7V	- .3V

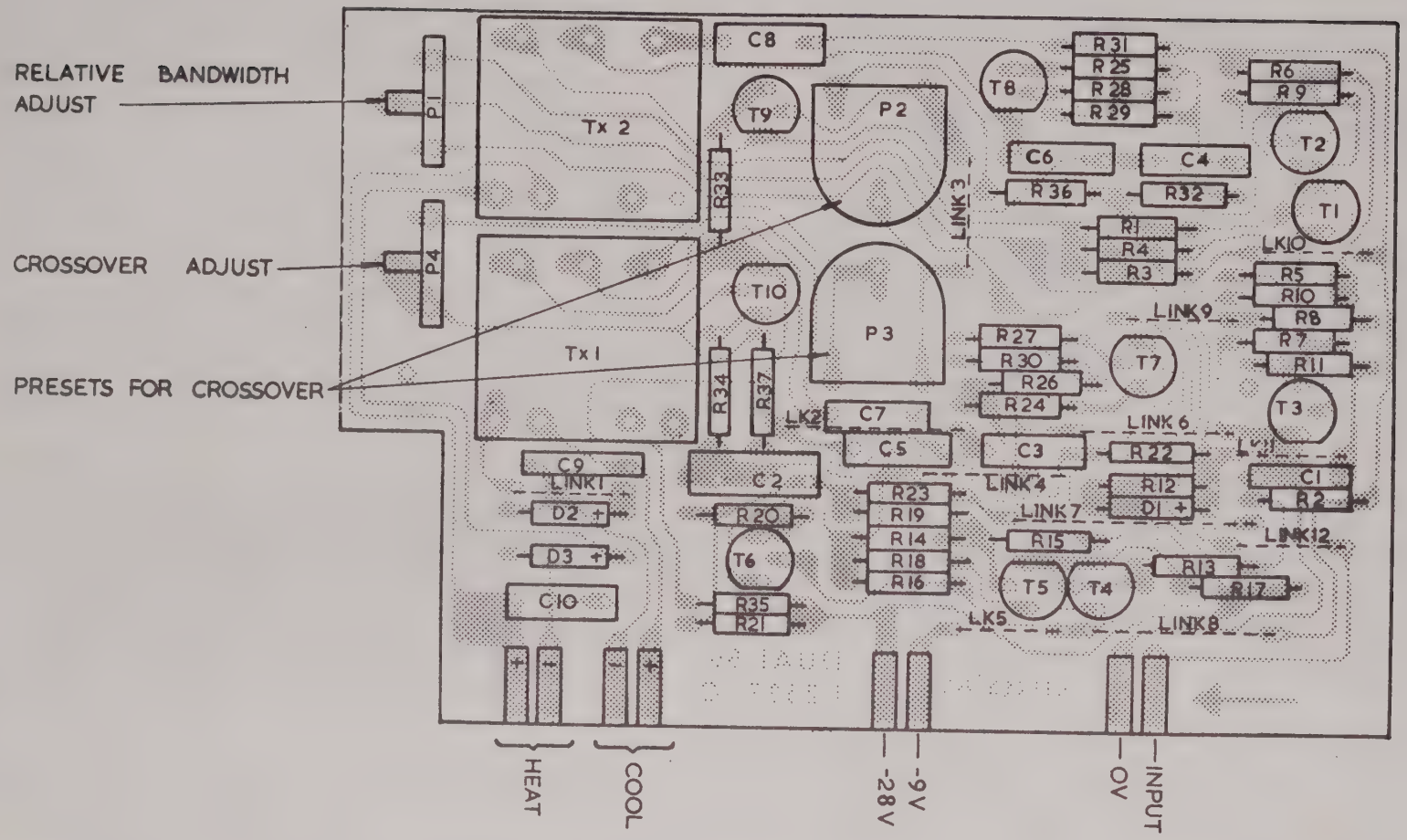
* Must be measured with an oscilloscope or electronic voltmeter due to high circuit resistance. All other measurements may be taken with a d.c. voltmeter having a resistance of 20KΩ/volt. All voltages measured with reference to 0V.



LAYOUT Nº D93254

LILLIPUT MkII.
DUAL 5v OUTPUT.

Drg Nº E92111 Sht 17.



Drg Nº D93254

CIRCUIT Nº E92111 Sht 17.

LILLIPUT MkII.
DUAL 5v OUTPUT.

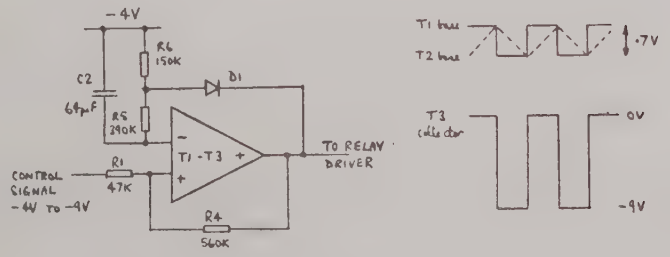
RELAY OUTPUT BOARD

Function

The relay output board converts a 0 to 5V d.c. input signal into a time proportioning relay output.

Circuit Description

The input control signal operates between the levels -4V and -9V, corresponding respectively to minimum and maximum relay ON time. Provision is made for reversing this action for cooling applications, the -4V and -9V input levels then corresponding respectively to maximum and minimum relay ON time. The output relay is energised on a time proportioning basis with an ON + OFF period of approximately 10 + 10 seconds at 50% output. For electrical heating applications power feedback is normally included so that the load power remains constant if the mains voltage varies. For cooling applications the power feedback feature is normally omitted. A spark suppression network can be provided across the normally-open output contact if desired.



Transistors T1 to T3 and associated components form a high-gain d.c. amplifier with overall positive gain from T1 base to T3 collector and positive feedback via R4. With an input control signal of -7V to R1, transistors T1 and T3 switch off and the collector of T3 falls to a potential of approximately -9V as defined by the current through T5, R11, D3, R17 when the board is operating in the normal mode. Positive feedback via R4 causes the potential at T1 base to fall to -7.2V. Diode D1 conducts, causing capacitor C2 to charge negatively towards -9V (T3 collector potential) via R5. When C2 has charged to -7.2V, transistors T1 and T3 conduct and T3 collector potential rises to 0V. Positive feedback via R4 causes T1 base potential to rise to -6.5V, ensuring that T1 and T3 remain hard on. Diode D1 is reverse biased and C2 commences to discharge towards -4V via R5, R6. Capacitor C2 discharges to -6.5V after approximately 10 seconds, at which point transistors T1 and T3 switch off. The positive feedback via R4 causes T1 base potential to fall again to -7.2V and capacitor C2 charges negatively from -6.5V towards -9V (T3 collector potential) via R5, D1. Capacitor C2 charges to -7.2V after approximately 10 seconds, at which point T1 and T3 conduct and the cycle is repeated. With an input control signal of -7V capacitor C2 thus charges and discharges continually between the levels of -6.5V and -7.2V producing a square wave of period approximately 10 + 10 seconds and magnitude approximately 9 volts at T3 collector. In the normal mode, with T4, R8, R9, D2 omitted and LK1 made, transistor T5 and the output relay switch ON whenever T3 collector is negative.

The ON-OFF switching differential of .7V at T1 base remains approximately constant as the input control signal varies, but the switching level follows the control signal. As the input control signal becomes more negative the average level of charge on C2 becomes more negative, causing the charging current via D1 to decrease and the discharge current to increase. This gives an increasing relay ON time and a decreasing relay OFF time until the output relay stays permanently ON when the control signal becomes more negative than T3 collector potential (approximately -9V). As the input control signal becomes less negative the output ON time decreases and the OFF time increases until the relay stays permanently OFF with an input control signal of less than -4V.

Power Feedback

Due to the square law relationship between voltage and power, a 10% rise in mains voltage will produce a 20% rise in load power with electrical resistance heating unless the output ON time reduces by 20% to compensate for the change. A 10% rise in mains voltage causes a 10% rise in the smooth, but unstabilised, -28V supply. This produces a 10% change in T3 collector voltage from -9V to -9.9V during the period when the output relay is ON. The increased charging current through R5, D2 reduces the output ON time by approximately 20% and thus compensates for the change in supply voltage. For correct mains voltage compensation in the normal mode, with T4, R8, R9 omitted and LK1 made, diode D2 must also be omitted. Inclusion of D2 in this mode will not remove power feedback but merely reduce it to an incorrect level.

Inverted Relay Mode

For cooling applications the mode of operation of the output relay can be inverted by including components T4, R8, R9, D2 and omitting LK1. When T3 collector falls to -9V, transistor T4 is switched on and the relay is de-energised. The relay energises when T3 collector rises to 0V and T4 becomes non-conducting. Inclusion of diode D2 clamps the junction R7, R18 at -9.5V and the correct feedback level of -8.5V at T3 collector is established by the potential divider R9, R18. Inclusion of diode D2 stabilises T3 collector potential against mains variations of the -28V supply and thus eliminates power feedback, this being an undesirable feature for cooling applications.

Relay Output Stage

Diode D4 provides a path for the inductive current of the relay coil when the relay is de-energised to protect T5 from excessive voltage. The spark suppression network consisting of filter C3, R15 and voltage dependent resistor R16 can be connected across the normally-open relay contact to absorb the inductive current of an external contactor coil. The second relay contact is used to operate the facia-mounted neons. In the normal mode the red neon illuminates when the relay is energised and the green neon

illuminates when the relay is de-energised.

Checking

1) With the output board and the main amplifier board inserted in the mother board, connect the mains supply and check the -4V, -9V, -24V and -28V supplies with a d.c. voltmeter. Failure of any of the power supplies could be due to a mother board or amplifier board fault.

2) Connect a 10V d.c. voltmeter between the control input and 0V terminals on the output board. Demand full power from the controller and check that the input control signal can be varied over the range -4V to -9V by adjusting the maximum power control P4 on the main amplifier board.

3) Set the input control signal to -6.5V and observe the operation of the output relay. The relay should cycle with an ON + OFF period of approximately 10 + 10 seconds and the red and green facia-mounted neons should light when the relay is energised and de-energised respectively. If the board is connected in the normal mode check that the relay ON time increases to maximum as the control input is increased to -9V and that the relay ON time decreases to minimum as the control input is reduced to -4V. If the board is connected in the inverted mode check that the relay ON time decreases to minimum as the control input is increased to -9V and that the relay ON time increases to maximum as the control input is reduced to -4V.

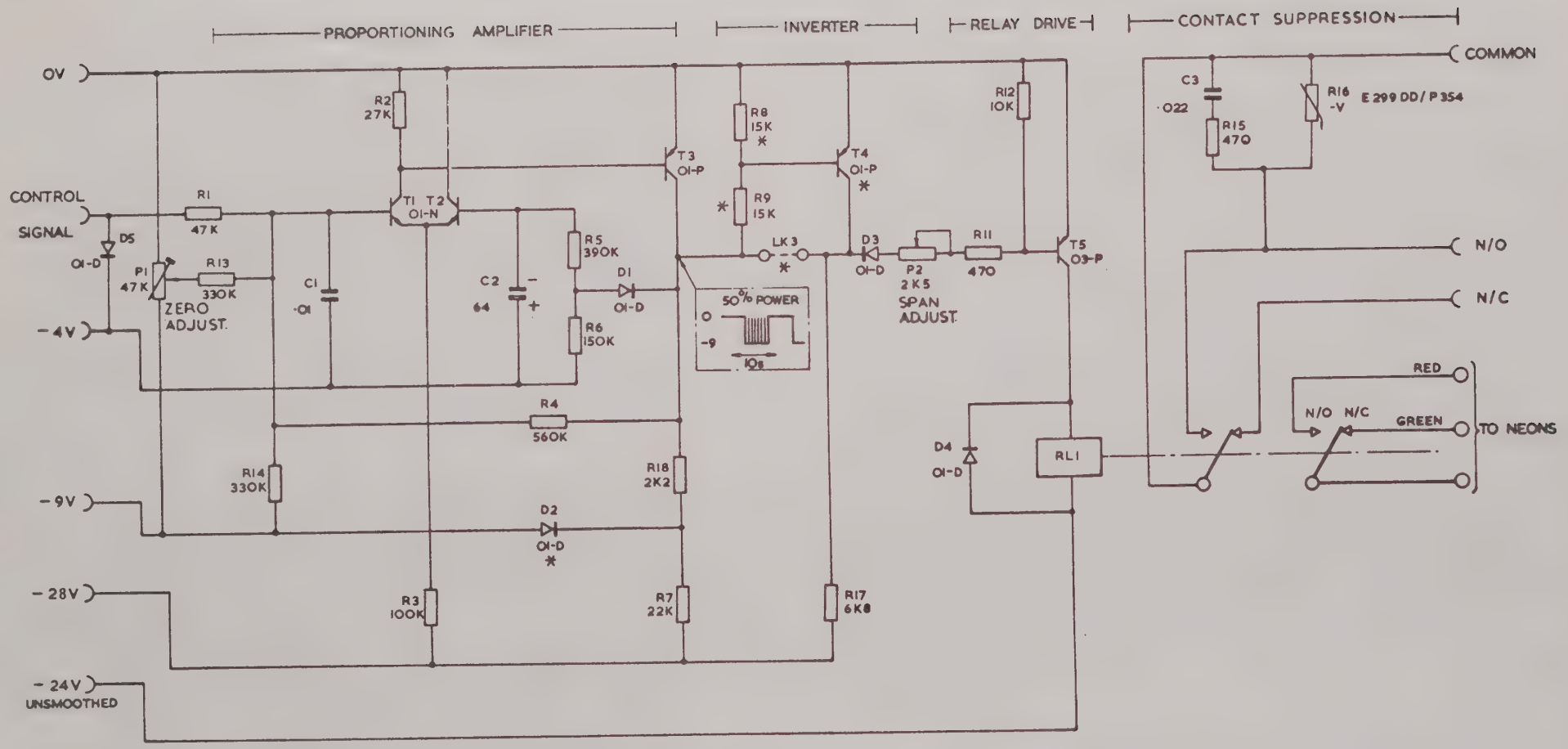
4) If the relay fails to cycle, set the control input to -6.5V and monitor the signal at T3 collector with the voltmeter. This signal should switch between 0V and -9V approximately once every 10 seconds. If this signal switches normally check operation of T5, RL1 or T4, T5, RL1 depending on the mode of operation. If the signal at T3 collector is not correct check operation of T1, T2, T3. The d.c. voltage table will assist in locating the fault.

D.C. Voltage Table

Typical d.c. test voltages for the two operating modes are shown in the table. With the output board and the main amplifier board inserted in the mother board, demand full power from the controller and set the maximum power control P4 on the main amplifier board to minimum and maximum respectively to set the two levels of control input.

	NORMAL					INVERTED	
	CONTROL INPUT	T1	T2	T3	T5	T4	T5
EMITTER	-4V	-4.5V	-4.5V	0V	0V	0V	0V
	-9V	-9V	-9V	0V	0V	0V	0V
BASE	-4V	-4V*	-4V*	-.7V	0V	0V	-.7V
	-9V	-9V*	-9V*	0V	-.7V	-.7V	0V
COLLECTOR	-4V	-.7V	0V	0V	-28V	-9V	0V
	-9V	0V	0V	-9V	0V	0V	-28V

* Must be measured with an oscilloscope or an electronic voltmeter due to high circuit resistance.
All other measurements may be taken with a d.c. voltmeter having a resistance of 20Kn/volt.
All voltages measured with reference to 0V.

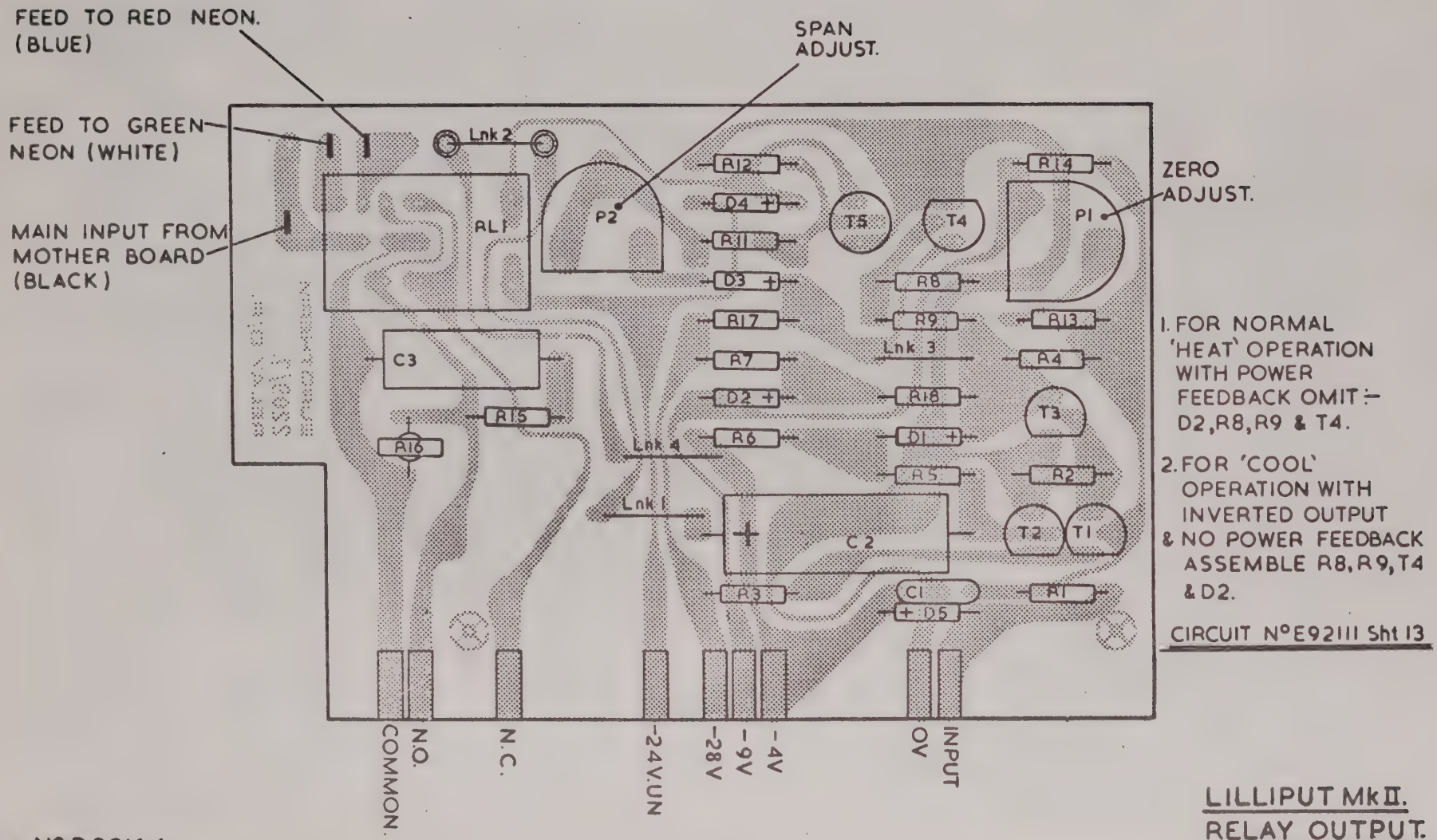


COMPONENTS MARKED THUS * VARY WITH MODE OF OPERATION.
FOR NORMAL OUTPUT, ASSEMBLE LK.3 & NOT R8, R9, T4.
FOR INVERTED OUTPUT, ASSEMBLE R8, R9, T4 & NOT LK.3
FOR POWER FEEDBACK OPERATION DO NOT ASSEMBLE D2.

LAYOUT Nº D93164

LILLIPUT Mk II.
RELAY OUTPUT.

Drg Nº E92111 Sht 13



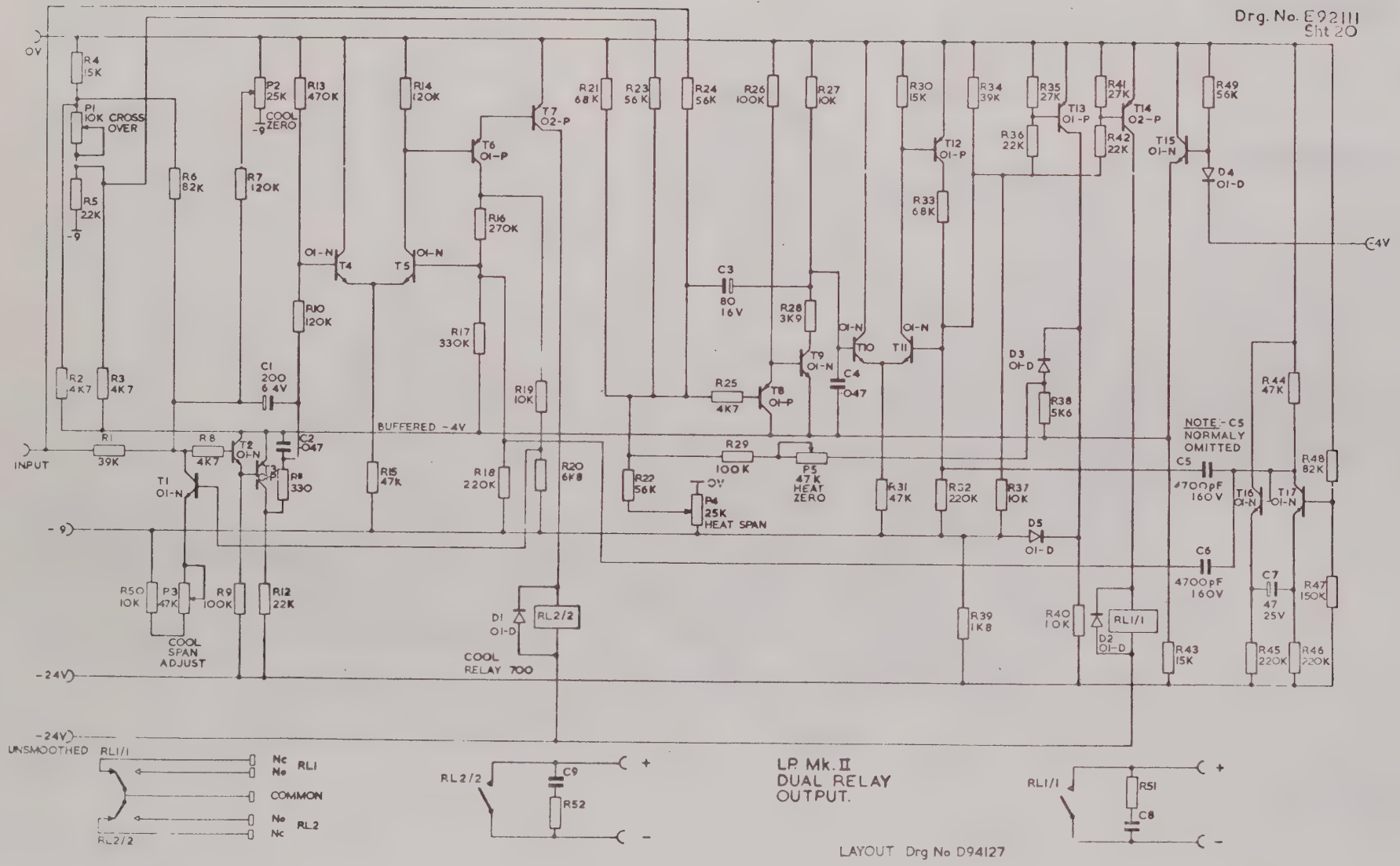
1. FOR NORMAL 'HEAT' OPERATION WITH POWER FEEDBACK OMIT :- D2, R8, R9 & T4.

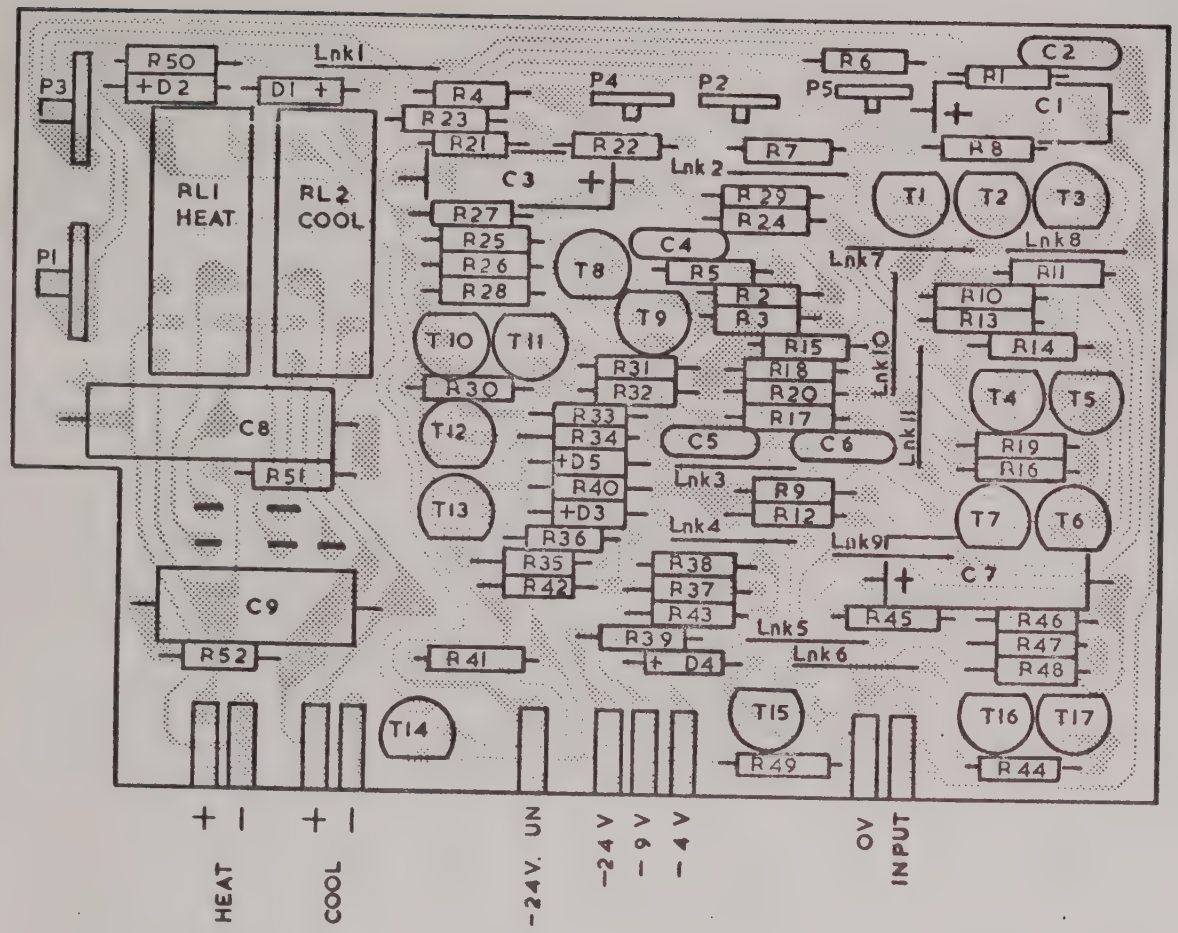
2. FOR 'COOL' OPERATION WITH INVERTED OUTPUT & NO POWER FEEDBACK ASSEMBLE R8, R9, T4 & D2.

CIRCUIT N°E92111 Sht 13

Drg N° D93164.

LILLIPUT Mk II.
RELAY OUTPUT.


Drg. No. E92111
Sht 20
0V
+4V
-9
-24V
INPUT
BUFFERED -4V
R1 39K
R2 4K7
R3 4K7
R4 15K
R5 22K
R6 82K
R7 120K
R8 4K7
P1 10K CROSS OVER
P2 25K COOL ZERO
R9 100K
R10 120K
R12 22K
R13 470K
R14 120K
R15 47K
R16 270K
R17 330K
R18 220K
R19 10K
R20 6K8
C1 200 6.4V
C2 047
C3 80 16V
C4 047
C5 4700pF 160V
C6 4700pF 160V
C7 47 25V
P3 47K COOL SPAN ADJUST
P4 25K HEAT SPAN
P5 47K HEAT ZERO
P8 330
R21 68K
R22 56K
R23 56K
R24 56K
R25 4K7
R26 100K
R27 10K
R28 3K9
R29 100K
R30 15K
R31 47K
R32 220K
R33 68K
R34 39K
R35 27K
R36 22K
R37 10K
R38 5K6
R39 1K8
R40 10K
R41 27K
R42 22K
R43 15K
R44 47K
R45 220K
R46 220K
R47 150K
R48 82K
R49 56K
R50 10K
R51
T1 01-N
T2 01-N
T3 01-P
T4
T5 01-N
T6 01-P
T7 02-P
T8 01-P
T9 01-N
T10
T11 01-N
T12 01-P
T13 01-P
T14 02-P
T15 01-N
T16 01-N
T17 01-N
D1 01-D
D2 01-D
D3 01-D
D4 01-D
D5 01-D
RL1/1
RL2/2
COOL RELAY 700
NOTE:- C5 NORMALY OMITTED
-24V UNSMOOTHED
Nc
No
RL1
COMMON
No
Nc
RL2
C8
C9
R52
LP Mk. II
DUAL RELAY
OUTPUT.
LAYOUT Drg No D94127



Lilliput MkII.

Dual Relay Output.

Circuit No F2111 Sht 20

DRG No D94127

ALL LIMITS BOARD

Function

The limits circuit provides operation of a relay at adjustable temperatures equally above and below the set point. The limits are adjustable between 1 and 10% of span.

Circuit Description

The output from the error amplifier is applied to the input of the positive variable gain feedback amplifier formed by transistors T1 to T3 and associated components. The output signal from this amplifier, taken from the junction of R5, R6, is applied to the hysteretic switching circuits formed by transistors T4, T5 and T6, T7. The relay RL1 is normally energised by conduction of T8. When the amplifier output reaches a level corresponding to either limit, as defined by P1 setting, hysteretic switching action causes T8 to switch off and the relay to de-energise.

The amplifier consists of a differential pair input stage T1, T2 and a single ended output stage T3. Negative feedback from the output at R5, R6 junction to the inverse input at T2 base via R3, P1 controls the amplifier gain. Potentiometer P1 provides adjustment of the limit setting.

With an error input of zero volts when the load temperature is at the set point, T6 conducts by virtue of the negative 1.5 Volt bias on T7 base (with respect to -4 Volts) provided by R20, R21, and supplies emitter current to the T4, T5 differential pair. Transistor T5 conducts by virtue of the +1.5 Volt bias on T5 base (with respect to -4 Volts) provided by R18, R19, and the relay is energised via D1 and T8.

As the load temperature increases towards the high limit, an increasing negative input is applied to T1 base. The amplifier output thus increases negatively and T6 conduction ceases as T6 base voltage increases negatively beyond T7 base voltage. As T6 is switched off, the emitter drive current to T4, T5 is removed and the relay is de-energised. In the high limit condition, positive feedback is applied to T6 base from T7 collector via R13 which holds T6 firmly off. The switching pair T6, T7 next change state, causing the relay to energise, only when the amplifier output rises sufficiently positive to overcome the hysteresis thus applied.

As the load temperature decreases towards the low limit, an increasing positive input is applied to T1 base. The amplifier output thus increases positively and T4 conducts as T4 base voltage increases positively beyond T5 base voltage. As conduction in T4 commences, T5 is switched off. Diode D1 therefore becomes non-conducting and T8 and the relay are switched off. In the low limit condition, positive feedback is applied to T4 base from T5 collector via R12 which holds T4 firmly on. The switching pair T4, T5 next change state, causing the relay to energise, only when the amplifier output falls sufficiently negative to overcome the hysteresis thus applied.

Diode D2 protects T8 from inductive voltage spikes produced by the relay coil. Capacitor C2 provides smoothing of the amplifier output signal and capacitors C3, C4 provide high frequency interference rejection. Capacitor C1 stabilises the feedback amplifier.

If the relay contacts are required to be closed at the set point and open in the alarm condition, link 2 must be made and link 3 omitted. If the relay contacts are required to be open at the set point and closed in the alarm condition, link 3 must be made and link 2 omitted.

Checking

1. With the limits board and the main amplifier board inserted in the mother board, connect the mains supply and check the -24V, -28V, +28V, -4V and -9V supplies with a d.c. voltmeter. Failure of any of the power supplies could be due to a mother board fault.

2. Set the control temperature to a value approximately mid-span and inject a corresponding signal into the thermocouple input from a millivolt source. With zero error, ensure that the relay is energised.

3. Set the limit alarm potentiometer P1 to approximately mid-way (5%). Slowly increase the injected millivolt signal to a value corresponding to 5% of span above the set point. Ensure that the relay de-energises at the alarm point.

4. Reduce the injected signal to a value corresponding to the set point. Check that the relay re-energises.

5. Reduce the injected signal to a value corresponding to 5% of span below the set point. Ensure that the relay de-energises at the alarm point.

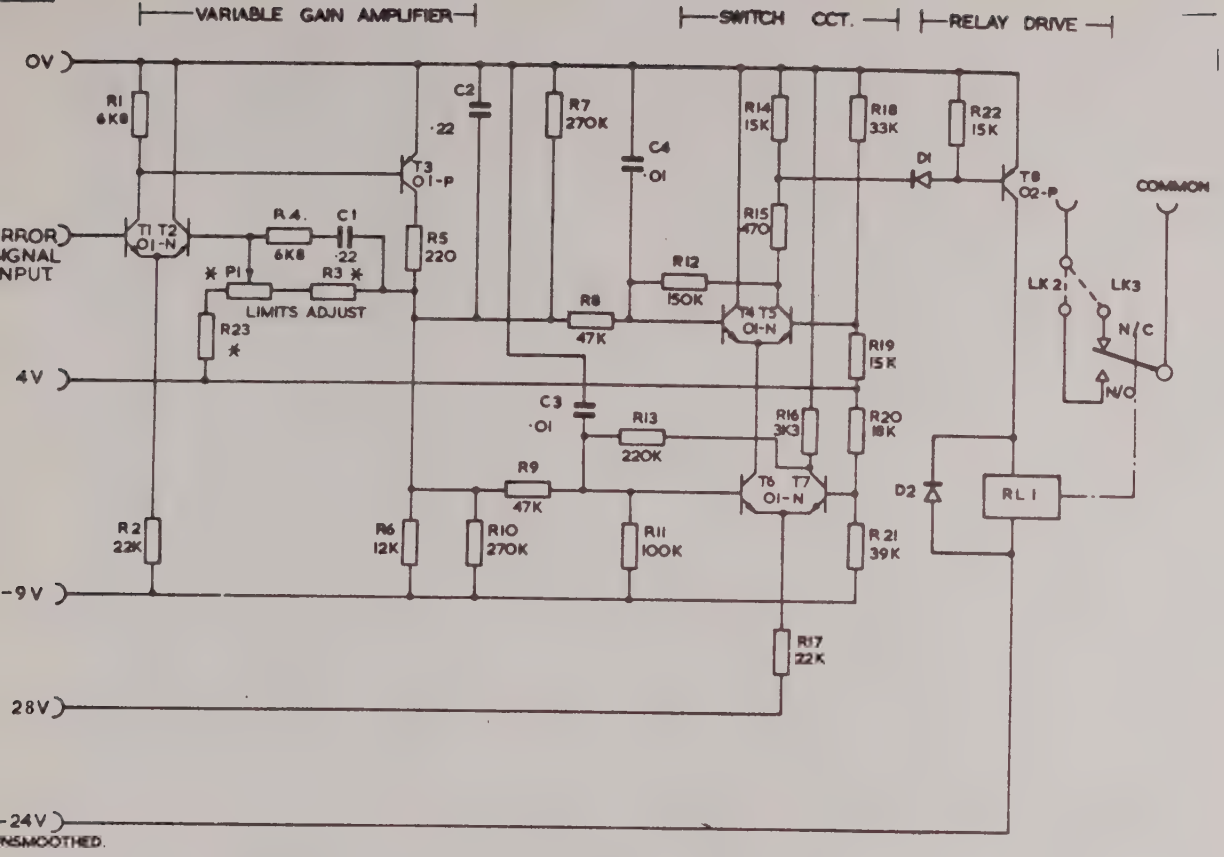
6. Check limit alarm operation at the two extreme settings of the limit potentiometer (1% and 10% of span). If the alarm is not functioning correctly, check the operation of T1, T2 and T3 with reference to the d.c. voltage table. If no fault is indicated, check the operation of T4 to T8.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to 0V using a d.c. voltmeter having a resistance of 20KΩ/Volt. The limit control P1 must be set to the maximum, fully clockwise position (10%). Voltages are checked with the indicator upscale (maximum over temperature error), downscale (maximum under temperature error) and at the set point (zero error).

	INDICATOR POSITION	T1	T2	T3	T4	T5	T6	T7	T8
EMITTER	UPSCALE (MAX ERROR)	-7	-7	0	0	0	-6	-6	0 V
	SET POINT (ZERO ERROR)	-4.5	-4.5	0	-3	-3	-5.5	-5.5	0 V
	DOWNSCALE (MAX ERROR)	-2.5	-2.5	0	-2	-2	-4	-4	0 V
BASE	UPSCALE	-6.5	-6	-ve	-4	-2.5	-6	-5.5	-ve V
	SET POINT	-4	-4	-0.5	-3	-2.5	-4	-5.5	-0.7 V
	DOWNSCALE	-2	-2	-0.5	-1	-2.5	-3	-5.5	0 V
COLLECTOR	UPSCALE	-ve	0	-6.5	0	-0.5	0	-3	-21 V
	SET POINT	-0.5	0	-4	0	-2	-3	-ve	0 V
	DOWNSCALE	-0.5	0	-1.5	0	-ve	-2	-ve	-19 V

Points designated only '-ve' are close to zero but slightly negative



COMPONENTS MARKED THUS * VARY WITH RANGE.
SEE WRITE UP FOR DETAILS.
LAYOUT Nº D93261.

LILLIPUT Mk II.
ALL LIMITS BOARD.

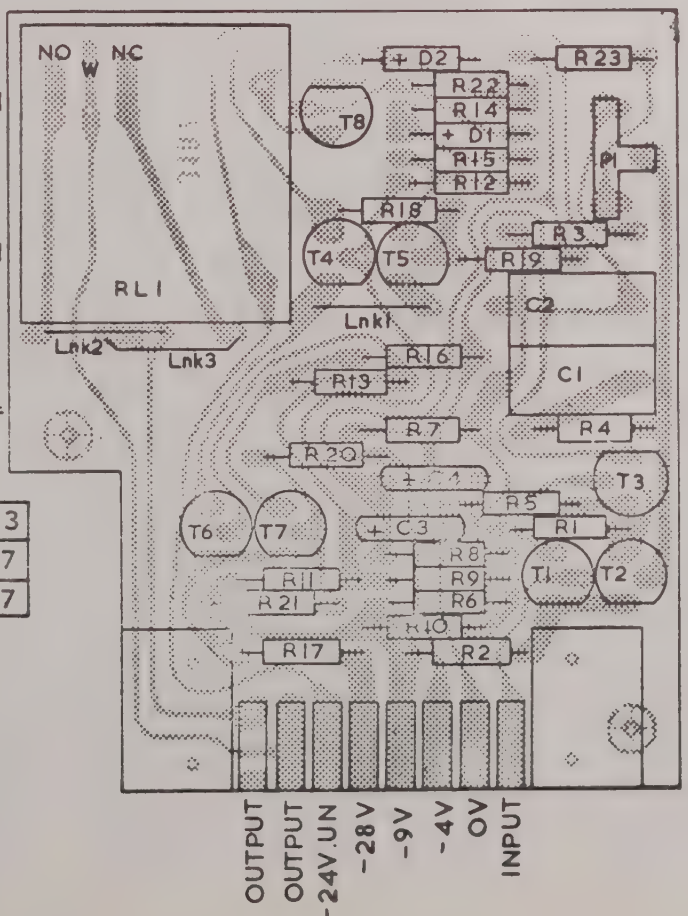
E92111 Sht 9 R

CONTACTS CLOSING
IN ALARM CONDITION
ADD LINK 3
OMIT LINK 2

CONTACTS OPENING
IN ALARM CONDITION
ADD LINK 2.
OMIT LINK 3

CIRCUIT Nº E92111 sht 9

RANGE	P1	R3	R23
0·5–5%	22K	33K	2K7
1–10%	22K	5K6	2K7



LILLIPUT Mk II.
ALL LIMITS.

Drg Nº D93261 R

HIGH/LOW LIMIT

Function

The limits circuit provides operation of a relay at adjustable temperatures above and below the set point. High limit operation occurs at temperatures above the set point and low limit operates below the set point. The limits are adjustable between 0 and 10% of span.

Circuit Description

The output from the error amplifier is applied to the input of the positive gain feedback amplifier formed by transistors T1 to T3 and associated components. The output signal from this amplifier, taken from the junction of R6, R7, is applied to the hysteretic switching circuits formed by transistors T4, T7 and T5, T6. The relay RL1 is normally energised by conduction of T8. When the amplifier output reaches a level corresponding to either limit, as defined by P2 setting, hysteretic switching action causes T8 and the relay to switch off.

The amplifier consists of a differential pair input stage T1, T2 and a single ended output stage T3. Negative feedback from the output at R6, R7 junction to the inverse input at T2 base via R5, P1 controls the amplifier gain. [redacted] potentiometer P2 provides adjustment of the base bias on T6 or T7 in the high or low limit modes respectively and determines the limit setting.

For high limit operation, only links 3, 5 and 6 are inserted and resistors R21, R22, R25, R26 are omitted. In the high limit mode, the amplifier output is fed to T4 base via R11 and link 6. With zero error input to T1 base when the load temperature is at the set point, T4 conducts by virtue of the greater negative bias on T7 base and supplies emitter current to the T5, T6 differential pair. Transistor T6 conducts and the relay is energised via D1 and T8.

As the load temperature increases towards the high limit, an increasing negative input is applied to T1 base. The amplifier output thus increases negatively and T4 conduction ceases as T4 base voltage increases negatively beyond T7 base voltage. The bias on T7 base is defined by the setting of potentiometer P2. As T4 is switched off, the emitter drive current to T5, T6 is removed and the relay is de-energised. In the high limit condition, positive feedback is applied to T4 base from T7 collector via R14 which holds T4 firmly off. The switching pair T4, T7 next change state, causing the relay to energise, only when the amplifier output rises sufficiently positive to overcome the hysteresis thus applied.

For low limit operation, only links 2, 4 and 7 are inserted with resistors R18, R19, R27, R28 omitted. In the low limit mode, the amplifier output is fed to T5 base via R10 and link 2. With zero error input to T1 base, when the load temperature is at the set point, T5 is non-conducting by virtue of the greater positive base bias on T6 base which holds T6 on. Diode D1 therefore conducts and the relay is energised via T8. As the load temperature decreases towards the low limit, an increasing positive input is applied to T1 base. The amplifier output thus increases positively and T5 conducts as T5 base voltage increases positively beyond T6 base voltage, the latter being determined by P2 setting. Conduction of T5 causes the relay to de-energise as D1 and T8 cut off. In the low limit condition, positive feedback is applied to T5 base from T6 collector via R13 which holds T5 firmly on. The switching pair T5, T6 next change state only when the amplifier output falls sufficiently negative to overcome the hysteresis thus applied.

Diode D2 protects T8 from inductive voltage spikes produced by the relay coil. The resistor chain R18 to R22 provides standing bias for T6 and T7. This bias is modified by an additional current bleed from the [redacted] limits potentiometer P2. Capacitor C1 provides smoothing of the amplifier output signal and capacitors C3, C4 provide high frequency interference rejection. Capacitor C2 stabilises the feedback amplifier.

If the relay contacts are required to be closed at the set point and open in the alarm condition, link 10 must be made and link 9 omitted. If the relay contacts are required to be open at the set point and closed in the alarm condition, link 9 must be made and link 10 omitted.

Checking

1. With the limits board and the main amplifier board inserted in the mother board, connect the mains supply and check the -24V, -28V, +28V, -4V and -9V supplies with a d.c. voltmeter. Failure of any of the power supplies could be due to a mother board fault.

2. Set the control temperature to a value approximately mid-span and inject a corresponding signal into the thermocouple input from a millivolt source. With zero error, ensure that the relay is energised.

3. Set the limit alarm potentiometer P2 to approximately mid way (5%). Note whether the board is connected for high or low limit. Slowly switch the injected millivolt signal to a value corresponding to 5% away from the set point towards the relevant limit. Ensure that the relay de-energises at the alarm point.

4. Return the injected signal to correspond to set point. Check that the relay re-energises.

5. Check the limit alarm operation at the two extreme settings of the limit potentiometer (1 and 10% of span). If the alarm is not functioning correctly, check the operation of T1, T2 and T3 with reference to the d.c. voltage table. If no fault is indicated, check the operation of T4 to T8.

D.C. Voltage Table

Typical d.c. test voltages for the transistors are shown in the table. All voltages are measured with reference to 0V using a d.c. voltmeter having a resistance of 20KΩ/Volt. The limit range control P1 must be set to approximately mid position (10%) and the limit control P2 must be set to the maximum fully clockwise position. Voltages are checked with the indicator upscale (maximum over temperature error) or downscale (maximum under temperature error) as appropriate, and with the indicator at the set point (zero error).

Low Limit Board

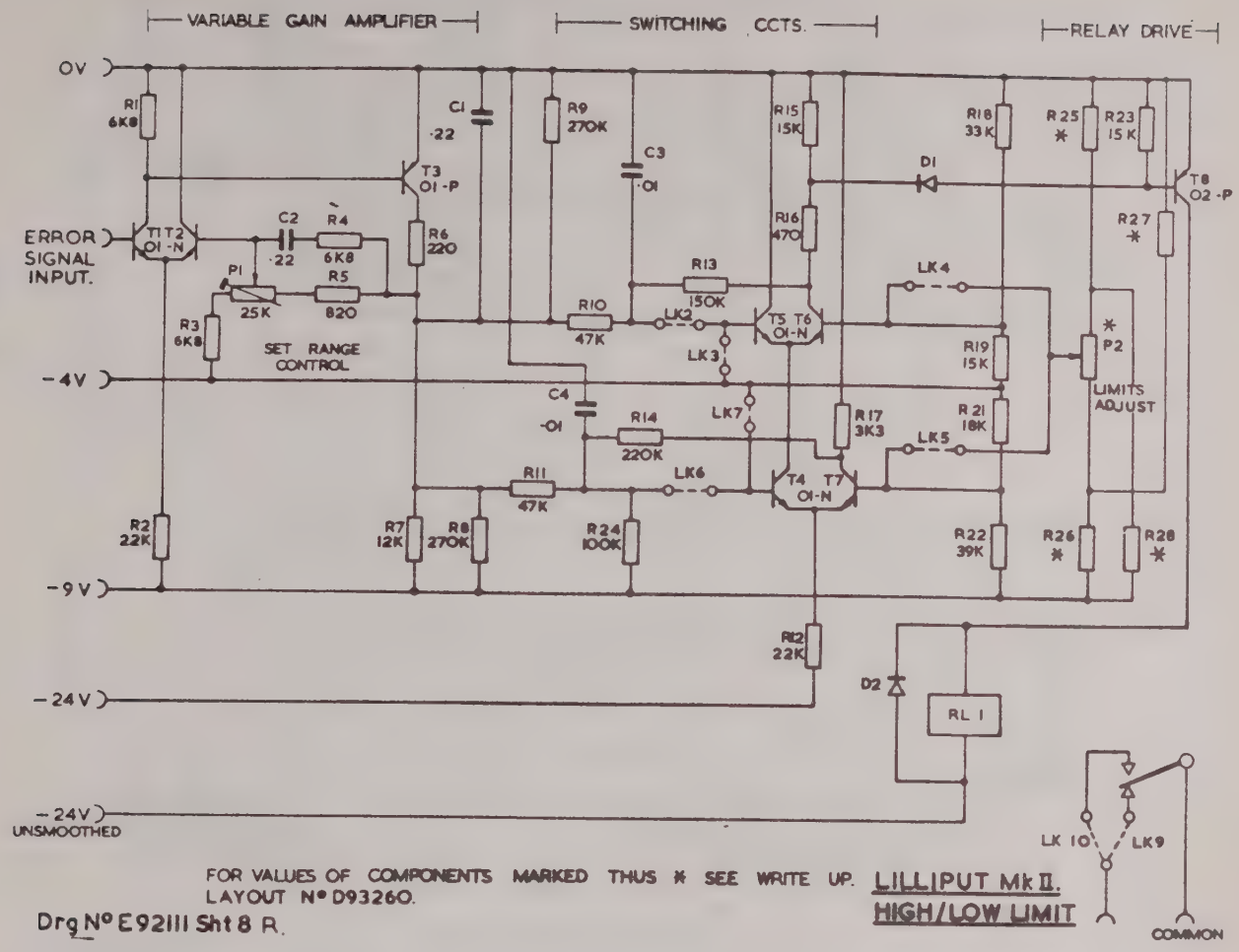
	INDICATOR POSITION	T1	T2	T3	T4	T5	T6	T7	T8
EMITTER	SET POINT (ZERO ERROR)	-4.5	-4.5	0	-4.5	-2.5	-2.5	-4.5	0 V
	DOWNSCALE (MAX ERROR)	-2.5	-2.5	0	-4.5	-1	-1	-4.5	0 V
BASE	SET POINT	-4	-4	-0.5	-4	-3	-2	-5	-1 V
	DOWNSCALE	-2	-2	-0.5	-4	-0.5	-2	-5	0 V
COLLECTOR	SET POINT	-0.5	0	-4	-2.5	0	-2	-ve	-ve V
	DOWNSCALE	-0.5	0	-0.5	-1	0	-ve	-ve	-20 V

Points designated only '-ve' are closed to zero but slightly negative

High Limit Board

	INDICATOR POSITION	T1	T2	T3	T4	T5	T6	T7	T8
EMITTER	UPSCALE (MAX ERROR)	-6.5	-6.5	0	-7	-ve	-ve	-7	0 V
	SET POINT (ZERO ERROR)	-4.5	-4.5	0	-5.5	-3.5	-3.5	-5.5	0 V
BASE	UPSCALE	-7	-6	0	-6	-4	-3	-6	0 V
	SET POINT	-4	-4	-0.5	-4	-4	-3	-6	-1 V
COLLECTOR	UPSCALE	0	0	-7	-ve	0	-0.5	-3	-21 V
	SET POINT	-0.5	0	-4	-3.5	0	-2	-ve	-ve V

Points designated only '-ve' are close to zero but slightly negative



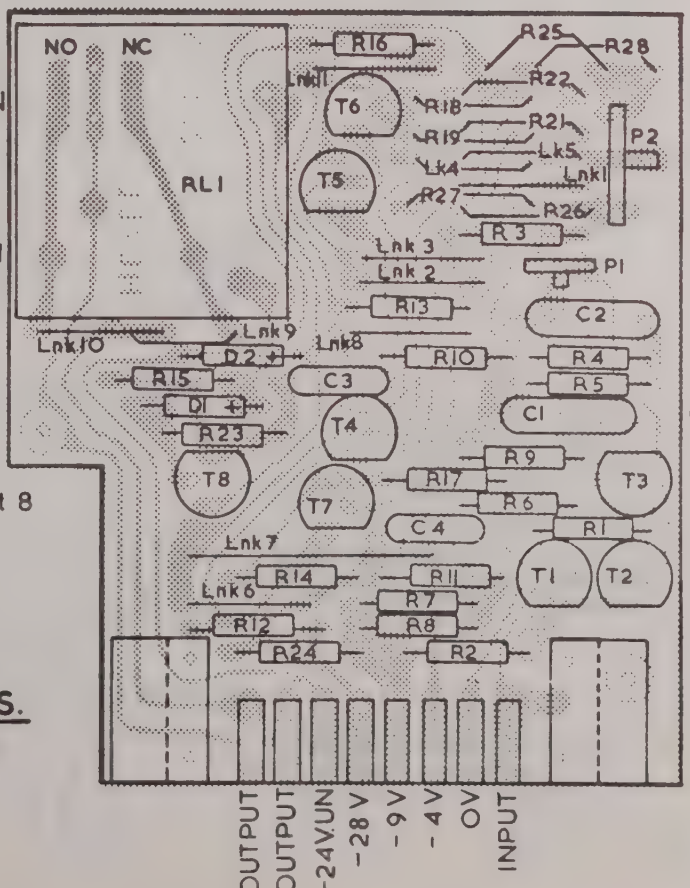
FOR VALUES OF COMPONENTS MARKED THUS * SEE WRITE UP. LAYOUT Nº D93260.

Drg Nº E92111 Sht 8 R.

LILLIPUT Mk II. HIGH/LOW LIMIT

CONTACTS CLOSING IN ALARM CONDITION
ADD LINK 9.
OMIT LINK 10

CONTACTS OPENING IN ALARM CONDITION
ADD LINK 10
OMIT LINK 9.



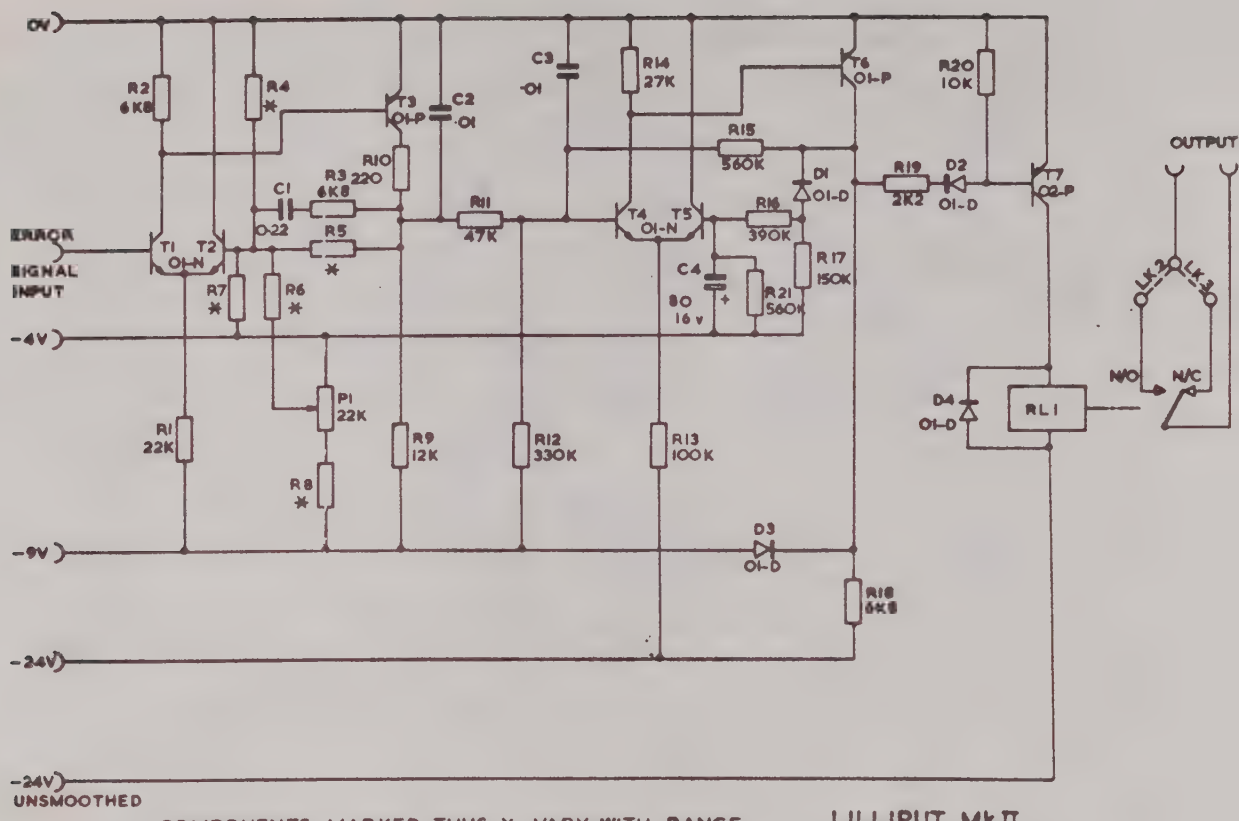
LINKS							
	2	3	4	5	6	7	
	—	√	—	√	√	—	
	√	—	√	—	—	√	

	R18	R19	R21	R22	R25	R26	R27	R28	P2	
HL	33K	15K	—	—	—	—	56K	—	22K	22K
LL	—	—	18K	39K	22K	56K	—	27K	22K	—

LILLIPUT Mk II. HIGH/LOW LIMITS.

CIRCUIT Nº E92111 Sht 8

Drg Nº D93260 R



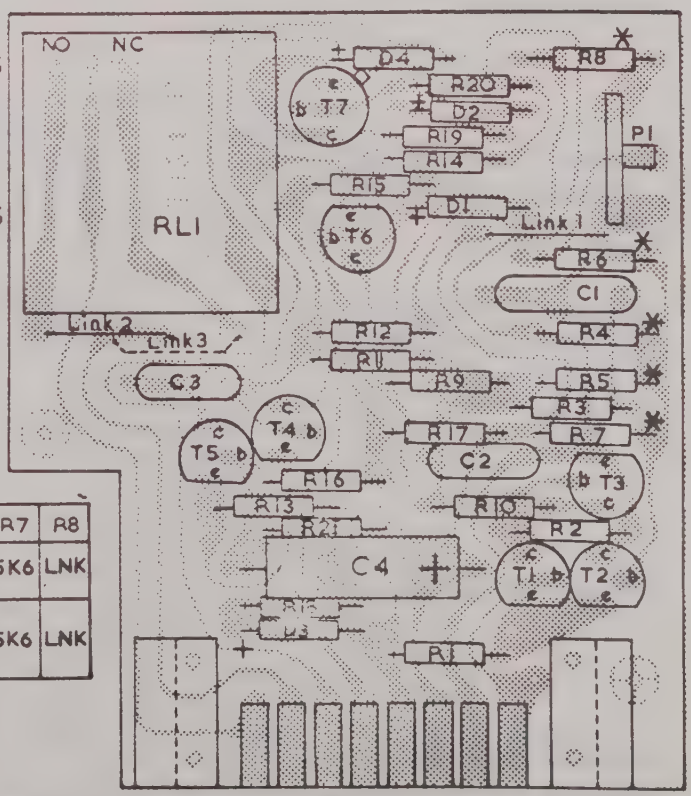
COMPONENTS MARKED THUS * VARY WITH RANGE.
SEE WRITE UP FOR DETAILS.
LAYOUT Nº D93925

LILLIPUT Mk II.
TIME PROPORTIONING
HIGH LIMIT.

R. E92111 Sht 18

* CONTACTS CLOSING
FOR HIGH TEMP.
ADD LINK 2
OMIT LINK 3

CONTACTS OPENING
FOR HIGH TEMP.
ADD LINK 3
OMIT LINK 2



RANGE	R4	R5	R6	R7	R8
4% PROP. O–5% SP'N	—	27K	39K	5K6	LNK
* 4% PROP. –6 TO +2% SPAN.	33K	27K	33K	5K6	LNK

OUTPUT
OUTPUT
-24V. UN
-24V
-9V
-4V
0V
INPUT

CIRCUIT Nº E92111 Sht 18.

* PREFERRED OPTION.

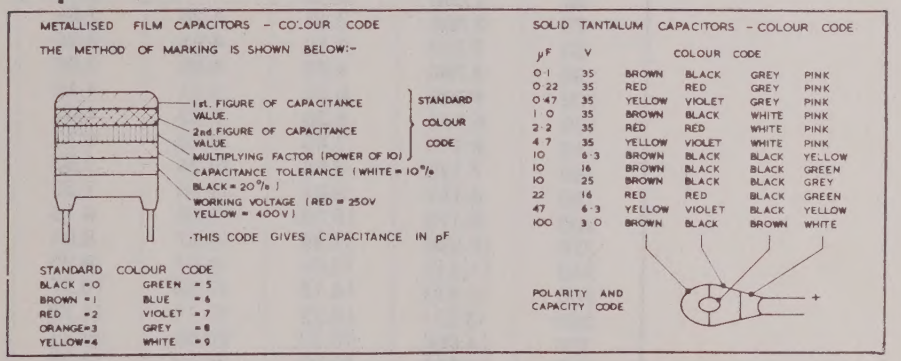
LILLIPUT Mk II
T.P.H.L.

Drg Nº D93925 R

Semiconductor Table

Circuit Reference	Commercial Equivalents
01–D	BAX16, IS922
01–N	BC168B, BC183LB
01–NF	2N 4303
01–P	BC258A, BC123LB
02–P	BC257A, BC212LB
05–N	BC131C
06–N	BC169B, BC184B

Capacitor Colour Codes


METALLISED FILM CAPACITORS - COLOUR CODE
THE METHOD OF MARKING IS SHOWN BELOW:-
1st. FIGURE OF CAPACITANCE VALUE.
2nd. FIGURE OF CAPACITANCE VALUE
MULTIPLYING FACTOR (POWER OF 10)
CAPACITANCE TOLERANCE (WHITE = 10% BLACK = 20%)
WORKING VOLTAGE (RED = 250V YELLOW = 400V)
STANDARD COLOUR CODE
·THIS CODE GIVES CAPACITANCE IN pF
STANDARD COLOUR CODE
BLACK =0 GREEN =5
BROWN =1 BLUE =6
RED =2 VIOLET =7
ORANGE=3 GREY =8
YELLOW=4 WHITE =9
SOLID TANTALUM CAPACITORS - COLOUR CODE
µF V COLOUR CODE
0·1 35 BROWN BLACK GREY PINK
0·22 35 RED RED GREY PINK
0·47 35 YELLOW VIOLET GREY PINK
1·0 35 BROWN BLACK WHITE PINK
2·2 35 RED RED WHITE PINK
4·7 35 YELLOW VIOLET WHITE PINK
10 6·3 BROWN BLACK BLACK YELLOW
10 16 BROWN BLACK BLACK GREEN
10 25 BROWN BLACK BLACK GREY
22 16 RED RED BLACK GREEN
47 6·3 YELLOW VIOLET BLACK YELLOW
100 3·0 BROWN BLACK BROWN WHITE
POLARITY AND CAPACITY CODE
+

COLOUR CODE FOR THERMOCOUPLE COMPENSATING CABLES

Thermocouple Type	Insulation Colour		
	Outer Sheath	Positive	Negative
Copper/Constantan	Blue	White	Blue
Nickel-Chromium/Constantan	Brown	Brown	Blue
Iron/Constantan	Black	Yellow	Blue
Nickel-Chromium/Nickel-Aluminium	Red	White or Red	Blue
Platinum-Rhodium/Platinum	Green	White	Blue

Reference Tables for Thermocouples

Reference junction at 0°C

°C	Cu/Con B.S. 1828: 1961	1/C B.S.1829 1962	NiCr Konst	C/A B.S. 1827 1952	Pt 10% RhPt B.S. 1826 1952	Pt 13% RhPt B.S. 1826 1952
0	0	0		0.00	0	0
5	0.193	0.25	.315	0.20	0.027	0.027
10	0.388	0.50	.630	0.40	0.055	0.054
15	0.584	0.76		0.60	0.083	0.082
20	0.783	1.02	1.25	0.80	0.112	0.111
25	0.984	1.28		1.00	0.142	0.140
30	1.188	1.54	1.86	1.20	0.172	0.170
35	1.393	1.80		1.40	0.202	0.200
40	1.600	2.06	2.47	1.61	0.233	0.231
45	1.809	2.32		1.81	0.265	0.263
50	2.021	2.58	3.06	2.02	0.297	0.295
55	2.234	2.85		2.23	0.330	0.328
60	2.449	3.11	3.66	2.43	0.363	0.361
65	2.666	3.38		2.64	0.396	0.395
70	2.885	3.65	4.28	2.85	0.430	0.429
80	3.329	4.19	4.91	3.26	0.499	0.499
90	3.780	4.73	5.55	3.68	0.570	0.570
100	4.239	5.27	6.21	4.10	0.642	0.644
120	5.176	6.36	7.52	4.92	0.791	0.796
140	6.140	7.45	8.86	5.73	0.945	0.955
160	7.129	8.56	10.24	6.53	1,104	1.119
180	8.142	9.67	11.65	7.33	1.268	1.289
200	9.178	10.78	13.08	8.13	1.435	1.463
220	10.236	11.89	14.57	8.94	1.605	1.641
240	11.315	13.01	16.07	9.75	1.778	1.823
260	12.413	14.12	17.59	10.57	1.954	2.010
280	13.531	15.22	19.11	11.39	2.133	2.199
300	14.666	16.33	20.65	12.21	2.314	2.392
350	17.580	19.09	24.59	14.29	2.777	2.886
400		21.85	28.60	16.40	3.249	3.397
450		24.61	32.65	18.51	3.730	3.921
500		27.39	36.75	20.65	4.220	4.460
550		30.22	40.82	22.78	4.719	5.010
600		33.11	44.94	24.91	5.226	5.571
650		36.08	48.99	27.03	5.742	6.146
700		39.15	53.03	29.14	6.265	6.735
750		42.32	57.02	31.23	6.798	7.338
800		45.53	60.95	33.30	7.339	7.952
850		48.73	64.85	35.34	7.888	8.576
900			68.61	37.36	8.446	9.209
950			72.34	39.35	9.014	9.853
1000				41.31	9.591	10.510
1050				43.25	10.172	11.176
1100				45.16	10.757	11.850
1150				47.04	11.348	12.532
1200				48.89	11.946	13.222
1300				52.46	13.155	14.617
1400					14.371	16.039
1500					15.580	17.463
1600					16.770	18.855